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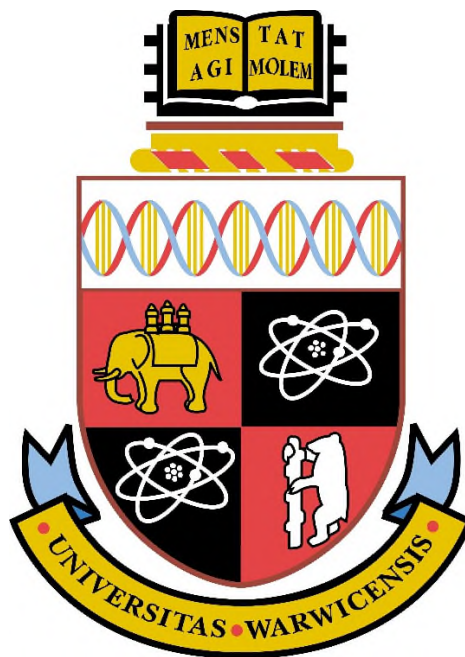
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Electrothermal Characterisation of Silicon and Silicon Carbide Power Devices for Condition Monitoring



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Dissertation submitted for the degree of
Doctor of Philosophy
July 2017

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Acknowledgements

To be honest, I am not a person inclined to give speeches, but as this section is here, I guess that I would have to prepare some words.

First, I would like to thank Layi Alatise, as supervisor on his efforts to delete the “I don’t know” from my mind and his guidance on this thesis.

Also, my gratitude to professors Li Ran and Phil Mawby for their help and support during this period of study, as well as boosting my confidence.

I would also like to acknowledge the support from everybody in the School of Engineering, University of Warwick, from the people in the office and the lab to the technicians. It has been a more or less long time since I started and some people are gone after they got a PhD, some people have left chasing new careers, some people are still around here and new people have arrived. To all of them my gratitude and admiration.

This research has been supported by the Centre for Power Electronics, Components Theme and Press-Pack Cross-Theme project. I would like to thank everybody I worked with, especially Dr. Attahir M. Aliyu from the University of Nottingham and Dr. Pushpa Rajaguru, from the University of Greenwich.

It is also good to remember where I started and where I am from, so I have to acknowledge my former colleagues at the University of Vigo. Some of them are still there, some have left, but we all meet in Christmas for our traditional lunch, to have a chat about power electronics and discuss a bit about our adventures around the world. Also, without the influence of them I would not be doing this.

As not everything is work, I would like to acknowledge the huge impact on my confidence that some people have had. People from the Coventry Godiva Harriers and the City of Coventry Swimming club, who encouraged me to run a marathon and swim. A mile fly a mile (or two) in Windermere.

Also, thanks to my landlord and family (a kind of new family in Coventry) for coping with the craziness of the last weeks while I was writing the thesis.

Finally, I would like to dedicate this work to my family. They are not physically here, but they have always been there. And my father, although he left us just one year ago, he will always with us. And I will always count up to thirty.

This work was supported by the UK Engineering and Physical Science Research Council (EPSRC) through the Underpinning Power Electronics Components Theme (EP/K034804/1) and HUB (EP/K035304/1).

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. It has been composed by myself and has not been submitted in any previous application for any degree.

The work presented (including data generated and data analysis) was carried out by the author except in the cases outlined below:

The structure functions presented in chapter 1 and chapter 5 were obtained at the University of Nottingham, where special power cycling and thermal impedance characterisation equipment is available, as required by the author.

The power cycling results presented in chapter 5 were obtained at the University of Nottingham, using special power cycling equipment, as defined by the author. The analysis of the results has been performed by the author of the thesis.

Parts of this thesis have been published by the author during the period of study, from April 2015 to July 2017. They are given in full detail in the Publication List section.

J. Ortiz González

July, 2017

Revised, October 2017

Abstract

Condition monitoring in power electronics is increasingly becoming a critical component of reliable power electronics both in traditional discrete and DBC packages as well as in pressure-packages. Condition monitoring involves on and off-line assessment of the state of health of the power module in an effort benchmark the reliability performance of the module (if off-line) or to prolong its useful operating life (if on-line).

One widely acknowledged method of condition monitoring involves the use of temperature sensitive electrical parameters (TSEPs) to estimate the junction temperature and hence, the junction to case thermal impedance as well as on-state electrical resistance. However, for TSEP based condition monitoring to become reality, a significant amount of electrothermal characterisation of modern power devices is necessary and that is where this thesis makes a valuable contribution, especially for new SiC power devices with relatively unknown thermal characteristics in alternative packages like press-packs.

TSEPs including diode/transistor on-state voltage drop, turn-on current switching rate, gate current/voltage switching transients etc., depend on the physics of the power devices and can vary from device to device depending on whether they are bipolar, unipolar, silicon or SiC. The on-state voltage drop of some devices exhibits a negative temperature coefficient, while others exhibit a positive one depending on the value of the Zero Temperature Coefficient (ZTC) point exhibited in the forward characteristics. The zero temperature coefficient results from the interaction between junction voltages which reduce with temperature (due to increased intrinsic carrier concentration from bandgap narrowing) and parasitic series resistances which increase with temperature (due to mobility and ambipolar diffusion length reduction with temperature).

This thesis shows that SiC power MOSFETs have the unique property of switching on faster at higher temperatures whereas the converse is true for silicon MOSFETs and IGBTs. Hence, the turn-on current switching rate has been proposed as a TSEP in SiC MOSFETs. The impact of parasitic inductance on the temperature sensitivity of the turn-on switching rate is also investigated and recommendations are made for the use of intelligent gate drivers with alterable gate driver impedances for implementing condition monitoring.

This thesis also investigates the impact of junction temperature variation in parallel connected power devices on the accuracy of the TSEP for the entire module and how the gate driver could be used to improve the temperature sensitivity of determined electrical parameters. In the context of pressure-packaged assemblies, where the thermal impedance is inextricably linked with the electrical impedance, this thesis presents the electrothermal characterisation of SiC Schottky diodes. Both a single chip and a multichip press-pack prototypes have been designed and tested, including the evaluation of different intermediate contact materials, namely Aluminium Graphite and molybdenum. The impact of pressure imbalance and device temperature characteristics (ZTC point) on electrothermal stability of parallel devices are explored in this thesis.

Publication List

Chapter 2

1. J. A. Ortiz Gonzalez, O. Alatise, N. Nobeen, J. Hu, L. Ran and P. Mawby, "Electrothermal Considerations for Power Cycling in SiC Technologies," presented at the 9th International Conference on Integrated Power Electronics Systems CIPS, Nuremberg, Germany, March 2016, pp. 1-6.
URL: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7736764&isnumber=7736696>

Chapter 3

2. J. Ortiz Gonzalez, O. Alatise, J. Hu, L. Ran and P. A. Mawby, "An Investigation of Temperature-Sensitive Electrical Parameters for SiC Power MOSFETs," in *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7954-7966, Oct. 2017.
doi: 10.1109/TPEL.2016.2631447
3. J. Ortiz Gonzalez, O. Alatise, J. Hu, L. Ran and P. Mawby, "Temperature sensitive electrical parameters for condition monitoring in SiC power MOSFETs," presented at 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, April 2016, pp. 1-6.
doi: 10.1049/cp.2016.026

Chapter 4

4. J. Ortiz Gonzalez, O. Alatise, L. Ran and P. Mawby "Impact of Temperature Imbalance on Junction Temperature Identification for Multiple Chip Modules Using TSEPs" presented at the PCIM conference, Nuremberg, May 2017
5. J. Ortiz Gonzalez and O. Alatise "Impact of the gate driver voltage on temperature sensitive electrical parameters for condition monitoring of SiC power MOSFETs," Accepted. To be published in a future issue of the journal *Microelectronics Reliability* and presented at the ESREF conference in September 2017.

Chapter 5

6. J. Ortiz Gonzalez, A.M. Aliyu, O. Alatisé, A. Castellazzi, L. Ran and P. Mawby, "Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules," in *Microelectronics Reliability*, Volume 64, 2016, Pages 434-439, ISSN 0026-2714, <http://dx.doi.org/10.1016/j.microrel.2016.07.062>. (Presented at the ESREF Conference, September 2016)
7. J. Ortiz Gonzalez; O. Alatisé; A. Aliyu; P. Rajaguru; A. Castellazzi; L. Ran; P. Mawby; C. Bailey, "Evaluation of SiC Schottky Diodes Using Pressure Contacts," in *IEEE Transactions on Industrial Electronics*, vol.PP, no.99, pp.1-1
doi: 10.1109/TIE.2017.2677348
8. J. A. Ortiz Gonzalez, O. Alatisé, L. Ran, P. Mawby, P. Rajaguru and C. Bailey, "An initial consideration of silicon carbide devices in pressure-packages," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7. doi: 10.1109/ECCE.2016.7854851
9. J. Ortiz Gonzalez, O. Alatisé, A. Castellazzi, A.M. Aliyu and P. Mawby, "Pressure Contact Multi-Chip Packaging of SiC Schottky Diodes," presented at the ISPSD conference, Sapporo, May 2017

Other publications

1. J. Ortiz Gonzalez et al., "Enabling high reliability power modules: A multidisciplinary task," presented at the 2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), Raleigh, NC, June 2016, pp. 1-5. doi: 10.1109/3DPEIM.2016.7570567
2. P. Rajaguru, H. Lu, C. Bailey, J. Ortiz-Gonzalez and O. Alatisé, "Electro-thermo-mechanical modelling and analysis of the press pack diode in power electronics," presented at the 21st International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Paris, September-October 2015, pp. 1-6.
doi: 10.1109/THERMINIC.2015.7389607
3. P. Rajaguru, J. A. Ortiz-Gonzalez, H. Lu, C. Bailey and O. Alatisé, "A Multiphysics Modeling and Experimental Analysis of Pressure Contacts in Power Electronics Applications," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 6, pp. 893-900, June 2017.
doi: 10.1109/TCPMT.2017.2688021

List of Acronyms

1G	First Generation
2G	Second Generation
3D	Three-dimensional
3L-NPC	Three level neutral point clamped
ALG	Aluminium Graphite
BJT	Bipolar Junction Transistor
CS-LCC	Current Source Line Commutated Converter
CTE	Coefficient of Thermal Expansion
DBC	Direct Bonded Copper
DC	Direct Current
DMOS	Double Diffused Metal Oxide Semiconductor
DUT	Device Under Test
EMI	Electromagnetic Interference
FACTS	Flexible Alternating Current Transmission System
FET	Field Effect Transistor
GTO	Gate Turn-off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
JFET	Junction Field Effect Transistor
LESIT	Leistung Elektronik Systemtechnik Informations Technologie
MMC	Modular Multilevel Converter
MMC	Metal Matrix Composite
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPC	Neutral Point Clamped
NPT	Non-Punch Through
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PCT	Phase Commutated Thyristor
PEEK	Polyether Ether Ketone
PPS	Polyphenylene sulfide

PTC	Positive Temperature Coefficient
PT	Punch Through
SC-VSC	Self-Commutated Voltage Source Converter
TSEP	Temperature Sensitive Electrical Parameter
TC	Temperature coefficient
UHVDC	Ultra High Voltage Direct Current
VD-MOSFET	Vertical Diffused Metal Oxide Semiconductor Field Effect Transistor T
ZTC	Zero Temperature Coefficient

Al_2O_3	Aluminium Oxide
AlN	Aluminium Nitride
GaN	Gallium Nitride
SF_6	Sulfur hexafluoride
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon oxide

List of Variables and Symbols

α_{pnp}	Current gain, pnp transistor
ΔT_j	Junction temperature variation
$\Delta t_{\text{plateau}}$	Variation of the time to plateau
A	Area, cross-section
A	Richardson's constant
c	Specific heat capacity
C	Capacitance, capacitor
C_{DC}	DC link capacitor
C_{DS}	Drain Source capacitance of a MOSFET
C_{GD}	Gate Drain capacitance of a MOSFET
C_{GD-HV}	Gate Drain capacitance of a MOSFET at high drain voltage
C_{GD-LV}	Gate Drain capacitance of a MOSFET at low drain voltage
C_{GS}	Gate Source capacitance of a MOSFET

C_{ISS}	Input capacitance of a MOSFET
C_{OX}	Gate oxide capacitance density
C_{th}	Thermal capacitance
C_{Σ}	Cumulative thermal capacitance
D	Diode
d	Separation between metal and semiconductor
d	Thickness, distance
D_a	Ambipolar diffusion coefficient
dI/dt	Rate of change of current with time
dI_{DS}/dt	Rate of change of the drain-source current with time
dI_F/dt	Turn-off current commutation rate
dI_R/dt	Reverse recovery switching rate
dR_{DS-ON}/dT	Variation of R_{DS-ON} with temperature
dV_{TH}/dT	Rate of change of the threshold voltage with temperature
E_C	Bottom edge of the conduction band
E_{FM}	Fermi level in the metal
E_{FS}	Fermi level in the semiconductor
E_G	Bandgap energy
$E_G(0)$	Bandgap energy at 0 K
E_V	Top edge of the valence band
g_{mS}	Saturation transconductance
I	Current
I_{DS}	Drain Source current of a MOSFET
I_G	Gate current
I_{GP}	Gate current plateau
I_{LOAD}	Load current
I_{RRM}	peak reverse recovery current
I_{SENSE}	Sensing current
J_C	Collector current density
J_{CH}	Channel current density
J_F	Forward current density
J_s	Saturation current density
k	Boltzmann's Constant
$K(R_{\Sigma})$	Differential structure function

L	Inductance
L_a	Ambipolar diffusion length
L_{CH}	Length of the channel of a MOSFET
L_S	Stray source inductance
n	Density of n-type carriers
N_A	Doping density
N_C	Density of states at the bottom of the conduction band
n_f	Number of cycles to failure
n_i	Intrinsic carrier concentration
N_V	Density of states at the top of the valence band
ϕ_{BN}	Schottky barrier height
ϕ_M	Work function of a metal
ϕ_s	Work function of a semiconductor
p	Density of p-type carriers
P	Power
Q	Transistor
q	Electron charge
R	Resistance, resistor
R_A	Accumulation resistance of a MOSFET
R_C	Electrical time constant
R_{CD}	Drain contact resistance of a MOSFET
R_{CH}	Channel resistance of a MOSFET
R_{CONT}	Resistance of a contact
R_{CS}	Source Contact resistance of a MOSFET
R_D	Resistance of a drift layer
$R_{D'-D}$	Parasitic resistance in the drain path
R_{DS-ON}	Drain-source resistance of a MOSFET in the on state
R_{EPI}	Resistance of the n- layer of a MOSFET
R_G	Total gate resistance
R_G^{EXT}	External gate resistance
R_{JFET}	JFET resistance of a MOSFET
R_{N+}	Source N+ resistance of a MOSFET
$R_{S'-S}$	Parasitic resistance in the source path
R_{SUB}	Substrate resistance

R_{th}	Thermal resistance
$R_{th,j-C}$	Thermal resistance junction to case
$R_{th,material-material}$	Thermal contact resistance between materials
$R_{TH}C_{TH}$	Thermal time constant
$R_{X(Material)}$	Electrical resistance of the element X, made of Material
R_{X-Y}	Electrical contact resistance between elements X and Y
R_{Σ}	Cumulative thermal resistance
S_A	Average surface roughness
T	Temperature
T_{AMB}	Ambient temperature
T_j	Junction temperature
T_{j-max}	Maximum Junction Temperature
T_{j-min}	Minimum junction temperature
T_m	Mean temperature
$t_{plateau}$	Time to plateau
t_{rise}	Rising time of the drain-source current
t_{TH}	Time to threshold
V	Voltage
V_{bi}	Built-in voltage of a pn junction
V_C	Contact potential
V_{drift}	Voltage across a drift region
V_{DS}	Drain Source Voltage of a MOSFET
V_F	Forward voltage of a diode
V_{FB}	Flatband voltage
V_G	Gate voltage
V_{GE}	Gate-emitter voltage
V_{GG}	Gate drive voltage
V_{GP}	Gate voltage plateau
V_{GS}	Gate Source Voltage of a MOSFET
V_{N+}	N+ junction voltage
V_{P+}	P+ junction voltage
V_S	Source voltage
V_{TH}	Threshold voltage
W_0	Width of the zero-bias depletion region

W_{cell}	Width of the cell of a MOSFET
W_{CH}	Channel width of a MOSFET
W_N	Thickness of the N-base region of an IGBT
W_d	Thickness of a drift layer
Z_{th}	Thermal impedance
β	Gain factor
ϵ_{Si}	Dielectric constant of Silicon
ϵ_{SiC}	Dielectric constant of Silicon carbide
λ	Specific thermal conductivity
μ_n	Electron mobility
μ_p	Hole mobility
μ_{ni}	Inversion layer mobility for electrons
ρ	Specific density
τ	Time constant RC
τ_{HL}	Carrier lifetime at high injection
χ_s	Electron affinity of the semiconductor
Ψ_B	Potential difference between Fermi Level and the intrinsic Fermi level

1 Introduction

1.1 Packaging of power semiconductor

Power electronic modules are comprised of power semiconductor devices mounted on packaging systems where heat extraction is a main design requirement. Power devices conduct electrical currents and block voltages thereby generating significant power losses. Because the performance of the power devices deviates from the expected performance at elevated temperatures, it is therefore necessary to control the average junction temperature of the power devices to guarantee normal operation, as well as limit the maximum junction temperature during operation. Hence, thermal management has played a fundamental role in power module design.

In typical power modules commercialised by mainstream vendors like Infineon, ABB, Fuji Electric, etc., the power semiconductor chips are mounted in an electrically isolated substrate comprised of copper and ceramic layers. The inter-layer dielectric (typically Al_2O_3 or AlN) is used for heat conduction and electrical isolation placed between 2 copper layers. This is the structure found in 70-80 % of the power modules manufactured in Europe and since the apparition of the first isolated power module in 1975 is the standard or classical packaging technique for a power module [1]. Figure 1.1 shows different power modules including the first isolated Semipack version and two modern Si IGBT and SiC half bridge power modules.

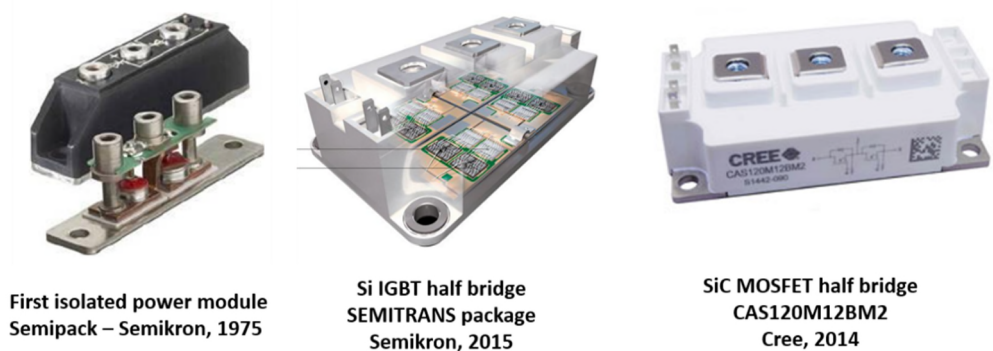


Figure 1.1 Different power modules with the traditional DBC structure [2-4]

Power modules can be manufactured with or without baseplates. Figure 1.2 (a) shows the cross-section of a power module with a baseplate while Figure 1.2 (b) shows a power module without a baseplate. The role of the baseplate is to increase the thermal capacitance of the cooling system, hence, it is used in power modules with higher power ratings. The use of the base plate also improves the mechanical strength of the power module, however a new solder layer is added to the system. Moreover, the use of a base plate adds two more elements to the thermal path, hence increasing the total thermal resistance of the module. In some cases, power devices may not be electrically isolated from the cooling system. A foremost example of this is series stacked pressure packaged power assemblies where the heatsinks also act as conducting poles.

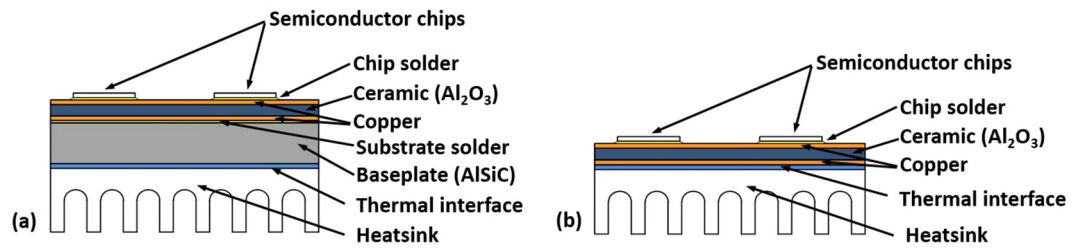


Figure 1.2 (a) Cross-section of a power module with base plate (b) Cross section of a power module without base plate. Adapted from [5]

The architecture of the classical power module, as shown in Figure 1.2, is comprised of different material interfaces. These include the semiconductor chip to copper layer interface through the solder (die attach), the copper layer to ceramic interface, the copper layer to baseplate interface and the baseplate to heatsink interface.

Each one of these materials has its characteristic thermal resistance and capacitance, hence, its specific thermal time constant. Furthermore, each material has its distinguishing coefficient of thermal expansion (CTE), hence, will mechanically respond to temperature changes in different ways. The differences in CTE cause tensile stresses at the material interfaces and over the life of the power module, the repeated power pulses will cause mechanical fatigue, as a result of the temperature variations during operation. The weak elements of the packaging are identified in red in Figure 1.3.

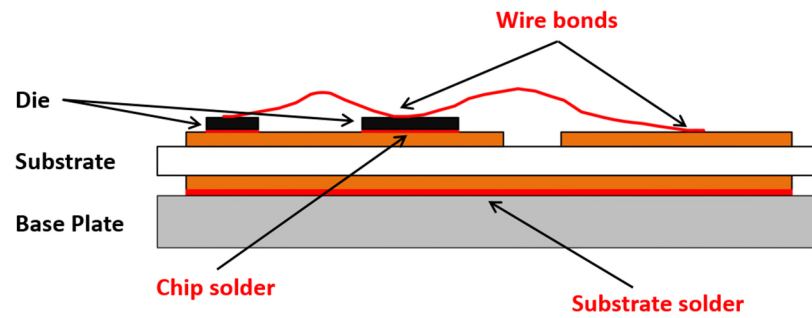


Figure 1.3 Weak elements of the classic power module structure, adapted from [5]

As cracks and voids emerge in the thermal interfaces, typically in the solder attaching the semiconductor chip to the substrate and the solder attaching the substrate to the baseplate, the ability of the module to extract the heat generated by the switching devices degrades. In other words, there is an increase in the thermal resistance of the power module. An example of cracks on the solder attaching the substrate to the base plate is shown in Figure 1.4

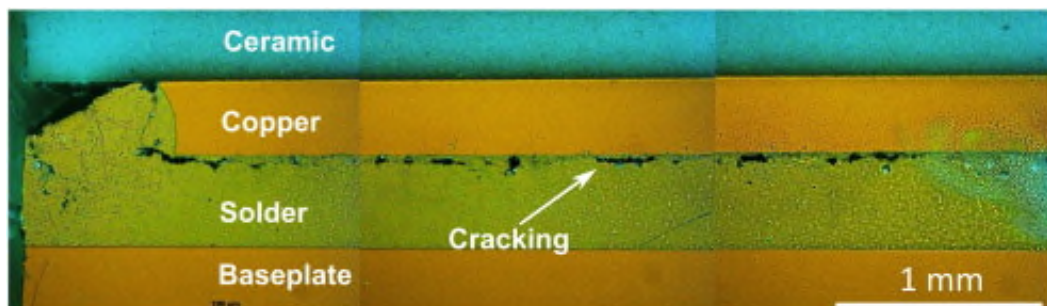


Figure 1.4 Cross-section of a power module with cracks on the substrate/base plate solder after power cycling [6]

Another weak element in the design of power modules is the source, emitter or anode wire bonds. These are the conductors that connect the top side of the power device to a conductive path in the copper substrate or the external package terminal, as well as the copper substrate to the external terminals. Wire bonding [7, 8] is a solid phase welding process to establish an electrical interconnection between a wire and a contact pad. A combination of heat, pressure and/or ultrasonic energy is used for attaching the thin wire to the desired surface (top side of the chip or substrate). The typical materials for the wire bond are gold and aluminium. Figure 1.5 [9] shows a typical example of a wire bond connected chip.

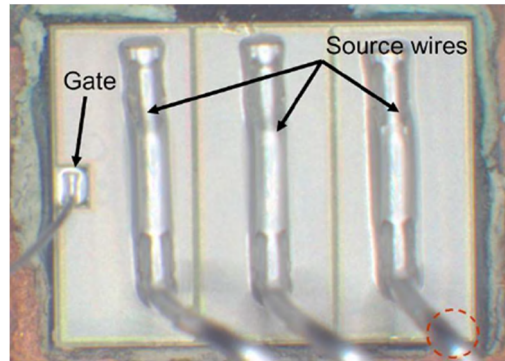


Figure 1.5 Example of the gate and source wire bond connections of a MOSFET [9]

These wire bonds are subject to thermo-mechanical stresses that arise from CTE mismatch and mechanical constraints [10]. Degradation in the contact resistance between the wire bond and the source metal leads to increased electrical resistance, which in turn leads to higher conduction losses. The wire bond can break partially or have cracks and, in the extreme case, a wire bond can lose all mechanical and electrical contact with the source metal, a failure mode known as “wire bond lift-off”. If all the wire bonds that are used in a connection lose electrical contact, the device fails into open circuit, which is a catastrophic failure for series connected devices. Metal reconstruction of the source contact arising from repeated thermal cycles can also contribute to increased source contact resistance [9]. Examples of metal wire bond damage and metallization reconstruction are shown in Figure 1.6.

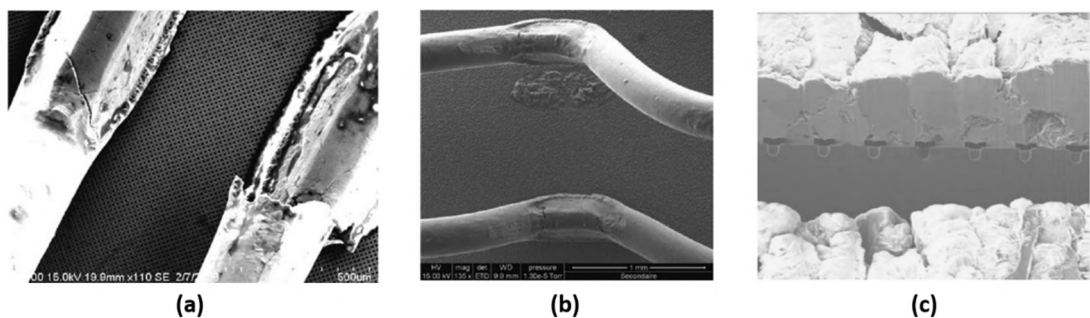


Figure 1.6 (a) Crack in a wire bond [10] (b) Wire bond lift-off [10] (c) Metallization reconstruction of the source of a MOSFET [9]

These degradation mechanisms are very well understood in the power electronics academic and industrial communities and several decades of academic and industrial research has been invested in understanding these mechanisms [1, 11, 12]. Innovations in

solder material chemistry, power module architecture, wire bond materials and design, etc.... have been developed over the last few decades [13]. Innovations in material science include copper wire bonds as a replacement to aluminium and silver sintering as alternative to conventional soldering. Innovations in power module architecture include double side cooling, flip-chip packaging, 3D packaging... Depending on the application of the power converter, the emphasis varies. For example, in power converters for electric vehicles, the size and weight of the cooling system is paramount for vehicle efficiency and range. In grid connected converters for HVDC/FACTS applications, the uniformity and effectiveness of the cooling system is paramount. Focusing on the semiconductor material, the packaging of wide bandgap semiconductors, like silicon carbide with different electrical and thermomechanical properties has also a new area of research for suitable packaging methods [14], for example, packaging suitable for high temperature and high frequency of operation which will not hinder the superior properties of the wide bandgap semiconductor.

1.1.1 Equivalent thermal models

As it was mentioned in the previous section, a power module comprises different materials which are in direct contact. The electrical properties of the selected materials as well as the thermal characteristics, together with the aforementioned coefficient of thermal expansion will have fundamental role on the design of the power module.

From the thermal point of view, a power module can be described using different equivalent circuit models [1, 15]. The Cauer model (also known as continued fraction circuit, T model or ladder network) is a representation of the physical configuration of the power module, where the thermal capacitances (C_{th}) and thermal resistances (R_{th}) are defined by the material properties of the materials. A 4-layer Cauer network model is represented in Figure 1.7, where the power dissipated is represented by a current source, the ground potential represents the ambient temperature and the thermal capacitances are connected to the ground.

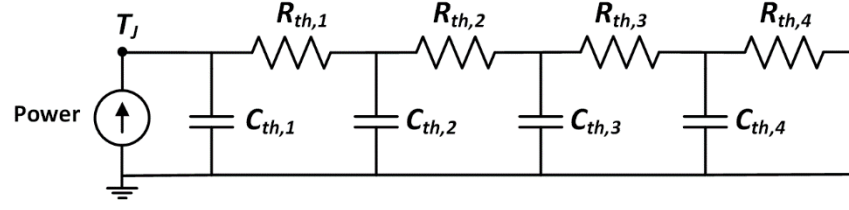


Figure 1.7 4-layer Cauer Network

The model presented in Figure 1.7 is a one dimension model, which assumes unidirectional heat flow, perpendicular to the cross-section of the material, without lateral heat spreading. Under this assumption, in a Cauer network, each of the RC levels can be assigned to a layer of the packaging system, with the thermal resistances and capacitances defined by the material properties. The values can be calculated using equations (1.1) and (1.2), where A is the cross-section of the material, d is the thickness of the layer, ρ the specific density, λ the specific thermal conductivity and c the specific heat capacity.

$$R_{th} = \frac{d}{\lambda \cdot A} \quad (1.1)$$

$$C_{th} = c \cdot \rho \cdot d \cdot A \quad (1.2)$$

The Cauer network model is physically correct, as it represents a physical model of the packaging system and each of the nodes can be assumed as physical locations within the packaging. On the other hand, the Foster network model (also known as partial fraction circuit or pi model) the RC elements do not represent any physical layer of the packaging system. Compared with a Cauer network, the capacitors of the network are connected in parallel to the resistors in the Foster model. A 4-layer Foster network is shown in Figure 1.8.

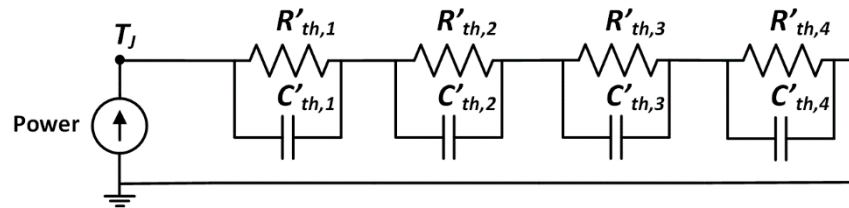


Figure 1.8 4-layer Foster Network

Both resistors and capacitors are different for the Foster and Cauer model networks presented in Figure 1.7 and Figure 1.8, however, the thermal transient response of the junction temperature is the same. Some particularities are that the RC pairs of a Foster network can be exchanged without modifying the transient thermal response of the system, opposed to a Cauer network, where the transient response will be affected. This is equivalent to a change of the physical layers of the package and underlines the missing link between a Foster network and the physical packaging, meaning that the material properties of the elements of the packaging cannot be used for determining the RC constants of the Foster network.

The importance of a Foster network is that it can be used for modelling the thermal impedance Z_{th} of the system using equation (1.3). The parameters R'_{th} and C'_{th} can be determined from a measured cooling curve, to match a particular heating or cooling curve. Some manufacturers of power modules list the values of these constants on the datasheets.

$$Z_{th} = R_{th}(t) = \sum_{i=1}^n R'_i \cdot \left[1 - \exp\left(-\frac{t}{\tau_i}\right) \right] \quad \text{where } \tau_i = R'_i \cdot C'_i \quad (1.3)$$

The one-dimensional Cauer thermal network is a simplification of the more complex power module, where the lateral thermal heat flux cannot be neglected. In order to model the lateral heat flow, three-dimensional thermal networks have been developed, extending the Cauer network to a three-dimensional model [1]. These models require powerful simulation tools, pre-processing and generation of the model of the power module to achieve adequate simulation results, nevertheless the three-dimensional analysis allows the identification of the temperature in points where the direct measurement is not feasible.

1.2 Reliability and lifetime

Temperature cycling [1] is a very important research and development tool that enables researchers and industrial manufactures of power modules ascertain the reliability and lifetime of power modules, being a requirement for qualification of power modules. Temperature cycling is an accelerated stress test which enables researchers to design

better power modules and test them ahead of deployment in the field. There are different types of temperature cycling tests, hence, it is important to understand the implications of the type of test used.

1.2.1 Passive temperature cycling and active temperature cycling

This is also referred to as temperature cycling. In this test, the power module is placed in a thermal chamber and the ambient temperature is cycled within defined temperature limits at a defined frequency. The cycle time and ramp rate is defined so that the temperature in the module is homogeneous, i.e. the module has reached thermal equilibrium and usually the rate of change of temperature is slow. For a fast change of temperature limits the test is named thermal shock test.

The power module is not electrically active, hence, this test is purely about controlling the ambient temperature. Typical temperature ranges are from -55 °C to 150 °C, but different standards have different requirements for application qualification. A final parameter check can be done to verify if the module has passed the test or intermediate measurements, can be performed to retrieve information regarding the electrothermal integrity of the power module.

Opposed to temperature cycling, in active temperature cycling, also referred as power cycling, the thermal stress is generated by the internal power dissipation of the devices in the module [16]. Hence, unlike passive power cycling test, the power devices in the module are electrically active, meaning that active power cycling tests not just the packaging but the device/package interaction.

1.2.2 Lifetime estimation

The test cycle is defined by the junction temperature swing (ΔT_j) and the medium temperature T_m , which are the parameters which will determine the number of cycles to failure n_f [1]. The duration of the cycle period will also have an impact on the elements of the packaging stressed in the tests. The number of cycles to failure n_f is the key reliability metric deduced from the power cycling tests.

$$\Delta T_j = T_{j-\max} - T_{j-\min} \quad (1.4)$$

$$T_m = T_{j-\min} + \frac{T_{j-\max} - T_{j-\min}}{2} \quad (1.5)$$

Failure is usually referred to as the point at which the thermal resistance of the power module increases by more than 20% compared to the untested module, however there are other electrical parameters which can also indicate a failure during power cycling, like an increase of the on-state voltage beyond the limit of 5% or 20%, loss the blocking capability of the device/module or the insulation between the gate and the emitter (IGBTs) or the gate to source (MOSFETs) [1]. By using accelerated stress tests and monitoring the thermal resistance of the power module at different intervals, the degradation process of the power module can be monitored and the lifetime of the power module can be predicted.

In the 1990s, the LESIT [1] project investigated the lifetime of IGBT power modules under power cycling. The number of cycles to failure (or lifetime) was characterised for different values of ΔT_j and T_m and the results were presented and summarised in [17]. From the experimental power cycling results, the number of cycles to failure is given by equation (1.6), where $A = 640$, $\alpha = -5$ and $Q = 7.8 \cdot 10^{-4} \text{ J} \cdot \text{mol}^{-1}$ for T_m in Kelvin and $R = 8.314 \text{ J/mol} \cdot \text{K}$. Equation (1.6) follows a Coffin-Manson model, where an Arrhenius factor has been included to indicate the impact of the medium temperature T_m on the lifetime results.

$$n_f = A \cdot \Delta T_j^\alpha \cdot \exp\left(\frac{Q}{R \cdot T_m}\right) \quad (1.6)$$

In 2008, an extended lifetime model was presented in [18]. In this study, the lifetime of traditional power modules was evaluated using experimental power cycling results considering different factors which can affect the lifetime. Among these parameters are the junction temperature swing ΔT_j , the minimum junction temperature T_{low} , heating time t_{on} , rated voltage of the chip V , diameter of the wire bond D and current per wire bond I , with the number of cycles to failure given by equation (1.7).

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{low}}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad (1.7)$$

The β_i parameters and K are determined from a set of experimental results and adjusted to obtain the best match and they are not physically independent [1, 18].

The impact on the lifetime of the voltage rating of the device is given by the thickness of the chip. For increasing the blocking capability of the devices, a thicker drift region is required, hence the global thickness of the chip increases. Results of power cycling of IGBTs rated from 600 V to 1700 V, with thicknesses ranging from 70 μm to 180 μm , are presented in [19], where a higher power cycling capability is observed for the thinner devices. However, in [18] the authors remark that this relationship between the power cycling capability and the thickness of the power device does not apply in the case of traction applications, given the different module setup and bonding technology.

The impact of a better manufacturing technology of the power module has been shown in [20], indicating how improvements in the wire bonds, the use of better attach methods, like diffusion solder and silver sintering, and improved substrates increases considerably the life time of the power modules.

In addition to lifetime models based on experimental data, the use of lifetime models based of physics-of-failure is an area where different research groups are active. Some of the research topics are the lifetime prediction of wire bonds [21] and solders [22].

1.2.3 Power cycling test methodology and power cycling control strategies

Active power cycling involves thermally excitation of the power module by electrical switching over a defined number of cycles and monitoring the thermal resistance evolution over time. It is widely acknowledged that high frequency power cycling tests (with short heating and cooling durations i.e. milliseconds) will stress the packaging components with the smaller thermal time constants ($R_{TH}C_{TH}$) while the lower frequency power cycling tests (with long heating and cooling periods i.e. hours/days) will stress the packaging components with long thermal time constants. An example of the

packaging component with a short thermal time constant is the wire bond, while one with a long thermal time constant is the module/base plate thermal contact.

Because the losses generated in the device are temperature dependent, and different power devices will dissipate different amount of losses, a defined control strategy is required for active power cycling. Four main control strategies for active power cycling can be identified [23], which will have an impact on the test results:

- a) **Constant Heating and Cooling Times Test.** Under constant heating and cooling times stress tests, a defined current is switched into the power device with a pre-defined duty cycle. Current is switched into the power device over a fixed duration to heat the device. As the current is switched off, the device cools down. The turn-on and turn-off durations are regardless of the state of health of the module, case temperature, temperature excursion etc. Hence, as the power device starts to exhibit increased thermal resistance from degraded thermal resistances between the critical interfaces, the failure accelerates since the test conditions remain unchanged and the average temperature increases.
- b) **Constant Case Temperature Excursion Test.** In this strategy of power cycling, the load current is controlled to keep the case temperature excursion constant. Unlike, the constant current test, the case temperature is monitored and the duty cycle of the heating current is varied so as to keep the case temperature excursion constant. A rise in the case temperature would be counter-acted by reduction in the pulse width of the heating current and a concomitant increase in the cooling duration. This test is less severe than the constant on-off times test.
- c) **Constant Power Test.** This test is based to the constant heating/cooling times test where the duty cycle of the device is fixed and the on-state and off-state times are regardless of case temperature. However, the difference is that the dissipated power is kept constant. This can be achieved by controlling the gate voltage in the case of MOSFETs and IGBTs. This test will typically start with a low gate voltage on the MOSFET/IGBT. This is introduce a higher than normal channel resistance, hence, a higher on-state voltage drop. As the module degrades as the losses increase together with the temperature, the gate voltage is reduced thereby causing

the off-state voltage drop to reduce. The result of this is that the power dissipation can be controlled and kept constant during the tests.

- d) Constant Junction Temperature Excursion Test.** In this variant of active power cycling methodology, the goal is to keep the junction temperature excursion constant during the whole duration of the test. This is usually done modifying the duty cycle of the heating current, hence the contribution of any degradation of the module to the junction temperature excursion during the test will be counteracted. Because the contribution of the module degradation to the device losses and junction temperature excursion is removed, this is the least stressful test and will result in the highest number of cycles to failure.

The four standard power cycling control strategies were defined for a traditional DC power cycling setup, which is the most common power cycling test circuit. Alternative test circuits have been proposed by different research groups, which are summarised in [16]. Among the proposed alternatives it is important to mention the back-to-back inverter configuration [24, 25]. Using this topology more realistic power cycling tests can be developed, as they can include the switching losses as well as conduction losses at the nominal rating of the power devices. However, this topology is not suitable for the testing of individual chips [16].

Another additional consideration regarding power cycling is that the aforementioned lifetime models have been obtained from the use of identical power cycles [1]. The design of power cycling tests based on a mission profile is an application oriented reliability test which can be useful for the determination of the lifetime in applications like railway traction [26], hybrid vehicles [27] or wind power converters[28]. This mission profile defines the operation of the power converter and generates a loss profile which will have an associated junction temperature profile, with different junction temperature excursions. These more complex temperature profiles require cycle counting algorithms together with linear accumulated damage assumptions [29]. The rainflow counting algorithm is one of the suitable approaches for counting temperature cycles generated by a mission profile [30].

1.2.4 Thermal impedance characterisation and structure functions

The structure function is a special function obtained from the transient cooling or heating curves using direct mathematical transformations [31]. This mathematical approach uses thermal resistances and capacitances in the Cauer form to identify changes in the thermal structure of the module and it has its importance in power cycling as it allows to study the module degradation during the tests if the thermal impedance is characterised [32].

Two types of structure functions are defined: differential and cumulative structure functions. The differential structure function, given by equation (1.8), is defined in [33] as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance, where a peak represents a new interface in the heat flow path.

$$K(R_{\Sigma}) = \frac{dC_{\Sigma}}{dR_{\Sigma}} \quad (1.8)$$

According to [33], for a slice of material of thickness dx and cross-section A , equation (1.8) can be calculated for a determined material with specific thermal conductivity λ and specific heat capacity c using equation (1.9).

$$K(R_{\Sigma}) = \frac{cAdx}{dx/\lambda A} = c\lambda A^2 \quad (1.9)$$

The cumulative structure function is the representation of the sum of the thermal capacitances as a function of the sum of the thermal resistances. When this structure function is discretised, it results in a Cauer network, which has a link to the real structure of the device, where a change in the slope represents a change of material.

Dedicated thermal impedance characterisation equipment [34], which can also perform power cycling, was used for obtaining the differential and cumulative structure functions of a discrete Schottky diode in a TO-247 package model C3D25170H from CREE/Wolfspeed. They are shown in Figure 1.9 and Figure 1.10 respectively.

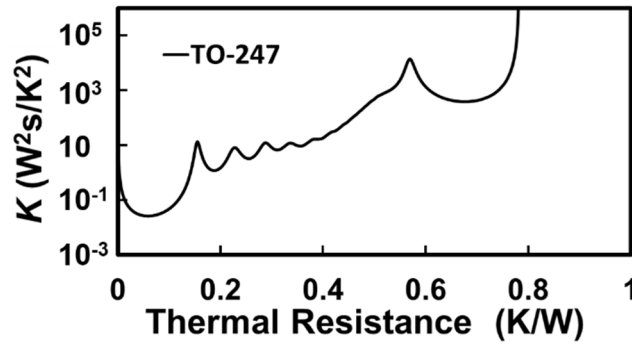


Figure 1.9 Differential structure function of a SiC Schottky diode in TO-247 package

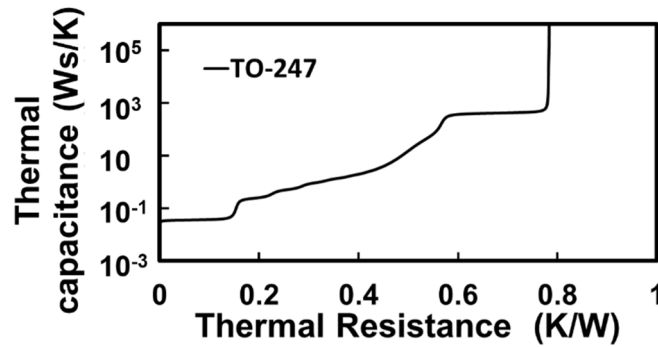


Figure 1.10 Cumulative structure function of a SiC Schottky diode in TO-247 package

This characterisation was performed in the University of Nottingham and from the structure functions presented in Figure 1.9 and Figure 1.10, the different elements of the packaging could be identified.

The thermal resistance was already an indicator of degradation, which was used by different researchers, for example [35], however the apparition of the state-of-art thermal characterisation and power cycling equipment [34] used for obtaining these structure functions has been fundamental for research on packaging systems and retrieving information from power cycling of power modules, as it allows to identify and monitor the degradation of the different layers of the power module, for example [6].

1.3 Condition monitoring

Power cycling is usually performed in a laboratory environment with controlled and defined test conditions. Power cycling tests are a valuable tool for obtaining lifetime estimation and designing better power modules.

As it has been already mentioned in this chapter, degradation of the packaging system and higher losses caused by unwanted operating conditions (overloading) will lead to a higher temperature of operation, hence the identification of the temperature would be a key element for implementing condition monitoring strategies, together with a suitable health management strategy.

Condition monitoring [36] consists in measuring the health state of a component, with the objective of taking the appropriate action if the condition of the component is degraded. It can be done on-line (during normal operation) or off-line (using a scheduled procedure). In order to implement an effective condition monitor system, understanding how the degradation of the module affects the electrical properties of the power module (for example wire bond lift-off and on-state voltage [37]) and how the operating conditions and packaging degradation affect the temperature of operation of the module is fundamental [38].

With an increasing demand of reliable power electronic systems, condition monitoring seems an optimal method for improving the reliability of the power modules. With SiC devices and power modules poised to replace their silicon counterparts, the requirement for electrothermal characterisation of SiC power devices is increasing. The reduced temperature sensitivity of SiC devices as a result of the wide bandgap, the use of multiple chips in parallel for increasing the current rating and packaging methods which can have an impact on the electrothermal characterisation require an extensive study and comparison with Si devices, especially for condition monitoring based on the use TSEPs.

1.4 Motivations and contributions

The primary motivation and contribution of this thesis is the electrothermal characterisation of modern silicon and SiC power devices for the purpose of laying the foundations of condition monitoring using temperature sensitive electrical parameters (TSEPs). Condition monitoring of power devices has become a very critical research topic in power electronics, especially since there is increasing conflict between power density and reliability especially in wide bandgap devices like silicon carbide. Condition monitoring simply refers to the ability to estimate the degradation of the device usually on-line without interfering with normal converter operation and take an appropriate action in case an issue is detected. A non-invasive technique of condition monitoring is based on measuring indirectly the on-line junction temperature of the power devices using temperature sensitive electrical parameters (TSEPs).

Condition monitoring based on junction temperature measurement will have several benefits including the aforementioned monitoring of the ageing of the power module during normal operation or power cycling. The ability to identify the operating junction temperature will also enable the definition of operative limits or constraints based on junction temperature and diagnosis of the performance of the device.

The use of these TSEPs require significant electrothermal characterisation and understanding, especially for SiC power devices which have different temperature dependencies compared with silicon. The implementation of condition monitoring based on junction temperature identification used TSEPs requires the evaluation of different TSEPs and selecting the most suitable for indirect junction temperature measurement. In the case of SiC power devices, the literature about TSEPs is limited and one of the contributions of this thesis is a thoroughly review of TSEPs for SiC power devices, including both dynamic and static TSEPs.

SiC power MOSFETs have the unique property of switching on faster at higher temperatures, hence this thesis proposes the switching rate during turn-on dI/dt as TSEP. For that end, the dependencies of dI/dt with parameters like the load current and the DC link voltage are analysed in this thesis. In addition, this thesis analyses the gate current plateau a TSEP together with the switching rate.

This thesis also presents a study of the effectiveness of TSEPs for parallel chips in the case of electrothermal imbalance. If condition monitoring using junction temperature estimation is used, this could be fundamental for detecting the aging of a power module with multiple chips in parallel.

Another contribution of this thesis to the end of condition monitoring is how the gate driver voltage could be used for improving the temperature sensitivity of determined TSEPs, like the proposed dI/dt . This contribution underlines the importance of intelligent gate drivers, capable of adjusting the gate resistance and output voltage, for enabling a more effective junction temperature estimation using TSEPs with augmented temperature sensitivity.

The reliability of the packaging system has been a concern of the power electronics engineers and packaging alternatives like pressure contacts have demonstrated an enhanced reliability due to the lack of solder and wire bonds. The packaging system selected will also have an impact on the condition monitoring strategy and this has been evaluated in this thesis using pressure contacts.

A final contribution of this thesis is the evaluation of the performance of SiC power devices using pressure contacts. For that end the prototype of a SiC Schottky diode using pressure contacts has been designed and tested. The use of alternative intermediate contact material (Aluminium Graphite) has been analysed together with the assessment of the performance of SiC Schottky diodes under power cycling. In addition, the impact of pressure non-uniformity between parallel chips and loss of contact pressure together with the electrothermal characteristics of SiC Schottky diodes have been evaluated and its implications on condition monitoring assessed.

1.5 Thesis outline

The main contents of the thesis are described below.

Chapter 2 of this thesis presents a review of TSEPs for different power semiconductor devices (including SiC Schottky Barrier Diodes, silicon MOSFETs, PiN diodes and silicon IGBTs), underlying the physics that governs the temperature sensitivity of the electrical parameters. Both static and dynamic TSEPs have been evaluated and the different experimental configurations for the electrothermal characterisation of power devices are presented in this chapter.

Si and SiC devices have different electrothermal properties and subjecting the devices to power cycling requires some preliminary considerations. A study of the impact on the power cycling performance of the different electrothermal characteristics of silicon PiN and SiC Schottky diodes concludes this chapter. Results in this chapter show that SiC Schottky diodes exhibit higher junction temperatures compared with silicon PiN diodes for the same current pulses. This is due to the lower zero temperature coefficient (ZTC) point in the diode forward characteristics in SiC Schottky diodes compared with silicon PiN diodes.

The results of this chapter have been presented at the CIPS conference in 2016.

Chapter 3 of this thesis investigates the temperature sensitivity of SiC power devices, starting with a general review of TSEPs for SiC power devices. The temperature sensitivity of SiC Schottky diodes and SiC power MOSFETs is evaluated for both dynamic and static TSEPs and compared with the silicon counterparts.

The on-state forward voltage at high and low temperatures is a well-known and well-established as TSEPs for silicon bipolar devices. While its use as a TSEP is feasible for SiC Schottky diodes, the reduced temperature sensitivity of the on-state resistance of SiC power MOSFETs compared to IGBTs makes the use of the measured forward voltage at low currents as a TSEP problematic. This chapter evaluates the turn-on current commutation rate (dI/dt) as a TSEP for SiC power MOSFETs. Using analytical modelling and experimental characterisation, the turn-on dI/dt is shown to have a unique temperature dependency not evident in other transistor technologies like silicon MOSFETs and IGBTs. In SiC MOSFETs, the turn-on dI/dt increases with temperature as a direct result

of the negative temperature coefficient (NTC) of the threshold voltage. In silicon MOSFETs, the NTC of the threshold voltage is counter-balanced by the mobility reduction at elevated temperatures whereas in IGBTs the NTC of the threshold voltage is overcome by the temperature dependency of the plasma formation in the drift region. Hence, the turn-on dI/dt is almost temperature invariant in silicon MOSFETs and reduces with temperature in silicon IGBTs. In SiC MOSFETs, the effective mobility of the carriers (and hence the channel resistance under full inversion) is not as temperature sensitive as is the case for silicon devices. Hence, SiC MOSFETs are unique in turning on faster at higher temperatures and thereby exhibiting reduced turn-on loss as temperature is increased.

For an effective condition monitoring using TSEPs, the good temperature sensitivity of the selected TSEP is a main requirement, hence this chapter presents a study of the temperature sensitivity of dI/dt as a function of the current rating of the device (size) and the nominal switching rate, determined by the gate resistance used. It is shown that the temperature sensitivity of dI/dt is more apparent for high current SiC MOSFETs, when they are driven using large gate resistances.

This chapter concludes with the analysis of the results for the implementation of condition monitoring using dI/dt as TSEP. The dependency of this TSEP on the DC link voltage and load current is evaluated and a list of different sensors for measuring dI/dt is presented.

The results in the chapter have been published in the IEEE Transactions on Power Electronics journal and presented at the IET Power Electronics Machines and Drives (PEMD) conference in 2016.

Chapter 4 of this thesis investigates the characteristics of TSEPs under the practical conditions of multiple die arrangements where devices are connected in parallel for high current conduction capability. This is done by using the forward voltage of silicon PiN diodes and SiC Schottky diodes as TSEPs. Electrothermal imbalance resulting from non-uniform degradation of the thermal resistances in parallel connected devices may impact the accuracy of the TSEPs in both silicon and SiC devices. The research presented in this chapter demonstrates the necessity of distinguishing between the individual temperature of the chips and the average/global temperature of the chips in the module.

In this chapter it is shown that the use of the traditional TSEP based on the forward voltage at low currents can lead to errors in the interpretation of the junction temperature, which can have negative consequences for condition monitoring. The distribution of the sensing current between the parallel chips is affected by the different temperature of the chips and it has been characterised in this chapter. It is shown that the sensing current flows mainly through the hotter device as the temperature difference increases and it has important implications on the junction temperature estimation. Investigations on the reverse recovery of parallel connected Si PiN and SiC Schottky diodes have also been performed in this thesis, together with the current distribution between the parallel chips at high currents. The reverse recovery is shown to be determined by the hotter device, hence it would be a good indicator of the maximum temperature.

The augmentation of the temperature sensitivity of the monitored parameter would be fundamental for enabling a more effective junction temperature estimation and this thesis investigates how the gate driver voltage can be used for maximising the temperature sensitivity of TSEPs for SiC power MOSFETs.

Regarding the on-state resistance, the thesis investigates how the gate driver voltage can be used to improve the temperature sensitivity of the on-state resistance (R_{DS-ON}) and how R_{DS-ON} as a TSEP depends on the specific channel design of the SiC MOSFET i.e. DMOS or Trench MOSFET designs. Using measurements, it is shown that different generations of SiC MOSFETs exhibit different R_{DS-ON} vs. temperature characteristics because of varying proportions of the channel and drift resistance as functions of the total on-state resistance. This chapter shows that a reduction of the V_{GS} can augment the temperature sensitivity of the R_{DS-ON} thereby improving its performance as a TSEP for condition monitoring in SiC power MOSFETs.

Considering the switching rate, studies presented in this chapter of the thesis show how driving the devices at low gate drive voltages has also an impact on the temperature sensitivity of the switching rate of dI/dt . It is shown that driving the MOSFETs using a low gate voltage increases the temperature sensitivity, as the impact of the lower threshold voltage on the transconductance is increased.

The results of this chapter have been presented at the PCIM Conference in Nuremberg (2017) and have been accepted for presentation at the European symposium

on reliability of electronic devices failure physics and analysis (ESREF) in 2017 and published in the Microelectronics Reliability journal.

Chapter 5 of this thesis investigates the performance of SiC power devices in pressure-packages and how the packaging system could have an impact on the junction temperature estimation and the condition monitoring strategy. The impact of intermediate thermal contact materials as well as that of pressure imbalance in parallel connected devices is investigated. Aluminium graphite and molybdenum intermediate contacts are compared for their electrothermal performances. The main contribution of this chapter is the demonstration of the importance of the zero temperature coefficient of the device in determining electrothermal stability of the power module. In pressure packaged power modules, pressure non-uniformity has been identified as a failure mechanism since it creates thermo-mechanical imbalance between the parallel devices. In press-pack IGBT power modules where several devices (transistors and diodes) are connected in parallel, pressure non-uniformity will cause the devices to have different junction-to-case thermal resistances as well as different electrical resistances. For there to be electrothermal stability, there must be a negative feedback loop between current and temperature i.e. the device that conducts more current by virtue of increased self-heating should become more resistance thereby reducing the current. The feedback mechanism is through the forward voltage. Below the ZTC, the forward voltage decreases with temperature (for the same current) whereas above the ZTC point, the forward voltage reduces with temperature (for the same current). If, however, there is a positive feedback loop between current and temperature, then the device conducting a higher current will continue to conduct more current since its increasing temperature reduces the forward voltage. SiC PiN diodes have higher ZTC points compared to SiC Schottky diodes and therefore, are more prone to electrothermal instability since a wider range of currents fall in the positive temperature coefficient range.

The results of this chapter have been published in the Microelectronics Reliability and IEEE Transactions on Industrial Electronics journals and have been presented at the ECCE conference (2016 in Milwaukee), International Symposium on Power Semiconductor Devices (ISPSD conference at Sapporo in 2017) and the ESREF conference (in Germany 2016).

1.6 References

- [1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2011.
- [2] T. Stockmeier, "From Packaging to "Un"-Packaging - Trends in Power Semiconductor Modules," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*, 2008, pp. 12-19.
- [3] Semikron. *SEMITRANS® 2-9 Power modules*. Available: <https://www.semikron.com/products/product-lines/semitrans/semitrans-2-9.html> (Access: 24/06/2017).
- [4] Cree/Wolfspeed. *CAS120M12BM2 1200-V, 13.0-mΩ, Silicon Carbide, Half-Bridge Module*. Available: <http://www.wolfspeed.com/cas120m12bm2> (Access: 23/06/2017).
- [5] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors* 2nd ed.: SEMIKRON International GmbH, 2015.
- [6] M. A. Eleffendi, L. Yang, P. Agyakwa, and C. Mark Johnson, "Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement," *Microelectronics Reliability*, vol. 59, pp. 73-83, 4// 2016.
- [7] Z. Lai and J. Liu. *The Nordic Electronics Packaging Guideline - Chapter A: Wire Bonding*. Available: <http://extra.ivf.se/ngl/A-WireBonding/ChapterA.htm> (Access: 24/06/2017).
- [8] Semikron. *Wire Bonding Technology*. Available: <http://www.powerguru.org/wire-bonding-technology/> (Access: 24/06/2017).
- [9] O. Alatise, I. Kennedy, G. Petkos, and A. Koh, "Reliability of Repetitively Avalanched Wire-Bonded Low-Voltage Discrete Power Trench n-MOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 1, pp. 157-163, 2011.
- [10] V. Smet, F. Forest, J. J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, *et al.*, "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4931-4941, 2011.
- [11] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 653-667, April 2002.
- [12] Semikron. *Failure Mechanisms During Power Cycling*. Available: <http://www.powerguru.org/failure-mechanisms-during-power-cycling/> (Access: 23/06/2017).
- [13] J. Schuderer, U. Drofenik, B. Agostini, F. Brem, F. Mohn, and F. Canales, "Challenges and new approaches for power module's next generation packaging technology," presented at the IMAPS From Nano to Micro Power Electronics and Packaging Workshop, 2013.

- [14] S. Seal and H. Mantooth, "High Performance Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions," *Energies*, vol. 10, no. 3, p. 341, 2017.
- [15] Infineon, "AN2008-3 Thermal equivalent circuit models," 1 ed, 2008.
- [16] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power Cycle Testing of Power Switches: A Literature Survey," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2465-2473, 2015.
- [17] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, 1997, pp. 425-430 vol.1.
- [18] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1-6.
- [19] A. Hensler, J. Lutz, M. Thoben, and K. Guth, "First power cycling results of improved packaging technologies for hybrid electrical vehicle applications," in *2010 6th International Conference on Integrated Power Electronics Systems*, 2010, pp. 1-5.
- [20] J. Lutz, "Packaging and Reliability of Power Modules," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-8.
- [21] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-Failure Lifetime Prediction Models for Wire Bond Interconnects in Power Electronic Modules," *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 1, pp. 9-17, 2013.
- [22] I. F. Kovacevic, U. Drofenik, and J. W. Kolar, "New physical model for lifetime estimation of power modules," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 2106-2114.
- [23] U. Scheuermann and S. Schuler, "Power cycling results for different control strategies," *Microelectronics Reliability*, vol. 50, no. 9, pp. 1203-1209, 2010/09/01/ 2010.
- [24] C. Oates, "Accelerated life testing of a traction inverter," *Power Engineering Journal*, vol. 13, no. 5, pp. 263-271, 1999.
- [25] F. Forest, J. J. Huselstein, S. Faucher, M. Elghazouani, P. Ladoux, T. A. Meynard, *et al.*, "Use of opposition method in the test of high-power electronic converters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 530-541, 2006.
- [26] L. N. X. Perpiñà, X. Jordà, M. Vellvehi, Jean-François Serviere and M. Mermet-Guyennet, "Reliability and Lifetime Prediction for IGBT Modules in Railway Traction Chains, Reliability and Safety in Railway," in *Reliability and Safety in Railway*, ed: InTech, 2012.
- [27] M. Ciappa, "Lifetime prediction on the base of mission profiles," *Microelectronics Reliability*, vol. 45, no. 9, pp. 1293-1298, 2005/09/01/ 2005.

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- [28] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590-602, 2015.
 - [29] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-8.
 - [30] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow Algorithm-Based Lifetime Estimation of Power Semiconductors in Utility Applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3368-3375, 2015.
 - [31] V. Székely and T. Van Bien, "Fine structure of heat flow path in semiconductor devices: A measurement and identification method," *Solid-State Electronics*, vol. 31, no. 9, pp. 1363-1368, 1988/09/01/ 1988.
 - [32] A. Aliyu and A. Castellazzi, "Prognostic System for Power Modules in Converter Systems Using Structure Function," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1-1, 2017.
 - [33] M. Rencz and V. Szekely, "Structure function evaluation of stacked dies," in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (IEEE Cat. No.04CH37545)*, 2004, pp. 50-54.
 - [34] Mentor. *Mentor Graphics T3ster*. Available: <https://www.mentor.com/products/mechanical/micred/t3ster/> (Access: 26/06/2017).
 - [35] A. Hensler, C. Herold, J. Lutz, and M. Thoben, "Thermal impedance monitoring during power cycling tests," presented at the PCIM Europe Conference, Nuremberg, 2011.
 - [36] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734-2752, 2010.
 - [37] J. Lehmann, M. Netzel, R. Herzer, and S. Pawel, "Method for electrical detection of bond wire lift-off for power semiconductors," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 333-336.
 - [38] M. A. Eleffendi and C. M. Johnson, "In-Service Diagnostics for Wire-Bond Lift-off and Solder Fatigue of Power Semiconductor Packages," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7187-7198, 2017.

2 Temperature sensitivity of power semiconductor devices and power cycling considerations

2.1 Introduction

The junction temperature is a key element in power cycling tests, life estimation and thermal impedance characterisation, however measuring the real time junction temperature of a power device is a very significant challenge in power electronics, one that many academic and industrial researchers are currently tackling.

If the power device is bare and not enclosed in a sealed power package, then it is possible to use infrared thermal cameras [1] to capture the surface temperature of the device. However, although this is possible in a laboratory set-up and it is a widely used technique for validation [2-5], deploying this in field operation is virtually impossible. Likewise, if it is a conventional power module, then it will most likely come enclosed in the module package. Chip temperatures can also be directly extracted using direct sensors integrated on the device during the fabrication process.-This method will require control of the power device fabrication as well as the module assembly process and the gate drive and control circuitry. However, this option is usually available for industrial organisations that fabricate power modules for dedicated applications like automotive and rail traction as well as industrial drives. In this case, these are usually not commercially available power modules since the industrial organisation fabricates them for in-house use. Examples of this include Toyota and Mitsubishi power modules designed for electric vehicle and rail traction respectively [6, 7].

The most widely recognised solution for junction temperature sensing during power cycling of semiconductor devices and modules is the use of Temperature Sensitive Electrical Parameters (TSEPs) [8-11]. TSEPs rely on the known temperature sensitivity of certain electrical parameters in power devices. The use of TSEPs involves monitoring the TSEPs and using calibration curves or look-up-tables to infer instantaneous device junction temperature. Most electrical parameters in power devices are temperature dependent. For instance, the breakdown voltage of diodes and transistors increases with temperature, the threshold voltage of transistors reduces with temperature, the on-state voltage of diodes and transistors changes with temperature etc. The next section of this

chapter delves into the physics behind the temperature sensitivity of different power devices.

2.2 Experimental configuration for the characterisation of TSEPs

Two different experimental configurations have been used in this thesis for the evaluation of TSEPs for different power devices. For the evaluation of static TSEPs, like the MOSFET on-state resistance or forward voltage at low and high currents of a diode, as will be evaluated later on this chapter, the circuit used is shown in Figure 2.1, while the experimental setup is presented in Figure 2.2.

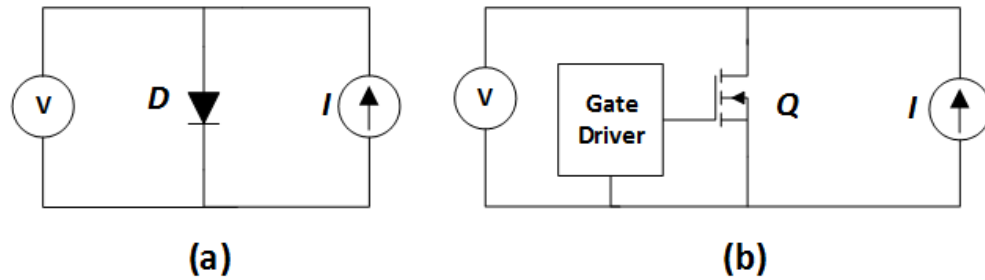


Figure 2.1 Electrical schematic for calibration of the on-state voltage as TSEP: (a) Diodes, (b) MOSFET/IGBT devices

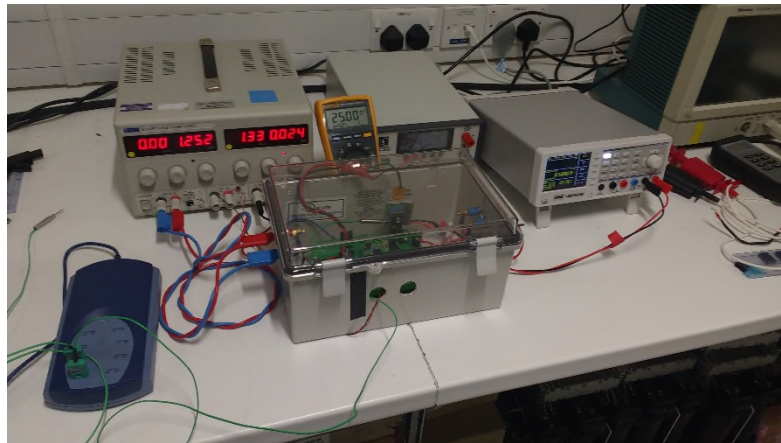


Figure 2.2 Experimental setup for the calibration of static TSEPs

A DC power supply which can operate in constant current mode is used for generating the current I which circulates through the device. This value of this DC current

can be low or high and it was measured using a digital multimeter Fluke 175. The low value current was generated using a power supply model EL302RT from TTI, while the high value DC was generated using a power supply model EA-PS5040-20 from Elektro-Automatik. The on-state voltage V was measured using a digital multimeter HAMEG model HMC8012 and the temperature was set externally using a small regulated DC heater, attached to the case of the discrete device. This temperature was captured using a thermocouple data logger model TC-08 from Pico Technology.

In the case of IGBTs and MOSFETs, as Figure 2.1(b) shows, a gate driver is used to apply a gate-to-source or gate-to-emitter voltage which will effectively turn on the device Q . The gate driver PCB used is shown in Figure 2.3 and it is based on the gate driver integrated circuit HCNW-3120. The supply voltage of the gate driver is generated using an isolated DC-DC converter 5 V/24 V and an adjustable voltage regulator LM317. Selecting a combination of resistors, the output voltage of the gate driver V_{GG} can be adjusted to the desired value. The schematic of the gate driver is described in the appendix of [12].

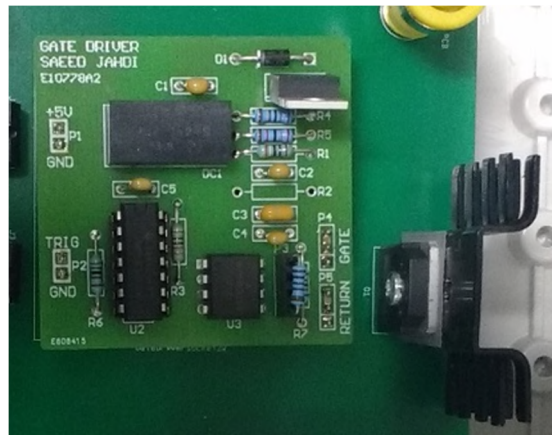


Figure 2.3 Gate driver board

A small DC heater was used for adjusting the temperature of the devices. A small block of aluminium was used to allow the connection of the discrete device to the heater, whereas a small block of copper was used to measure the case temperature of the device. The heaters used require a low voltage DC power supply (12-24 V) and they are self-regulated. They are manufactured by DBK Enclosures and are available in different power ratings, from 15 W to 60 W [13]. A detail of the assembly of the heater is shown in Figure 2.4.

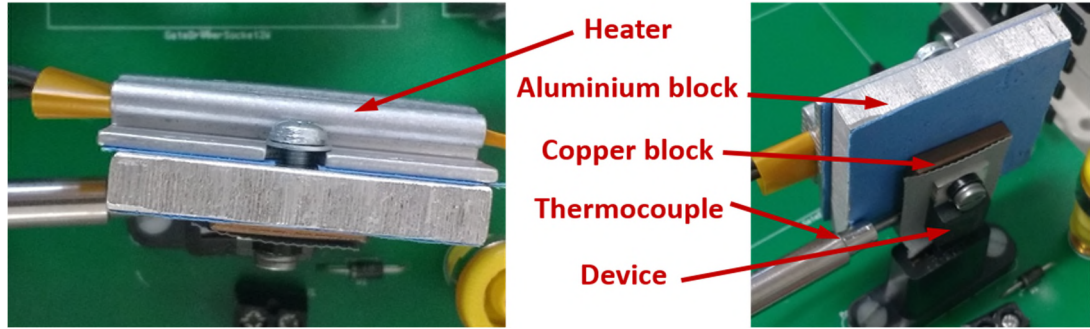


Figure 2.4 Detail of the DC heater assembly

The impact of temperature on the dynamic TSEPs can be evaluated using a traditional double pulse test set-up [14, 15] like the one shown in Figure 2.5, which is widely used for the dynamic characterisation of power semiconductors [16-18]. The electrical schematic and the test rig used are presented in Figure 2.5 and Figure 2.6 respectively. The operating temperature of the devices under test, which can be the diode D_I or the transistor Q_I , is controlled using a small temperature controlled heater attached to the discrete device, as described previously. The output voltage of the gate driver is adjusted to the required V_{GG} and the passive elements of the circuit are a 2 mH inductor L and a 470 μ F DC link capacitor C_{DC} . The power supply used is a 3000 W 720 V/15 A DC power supply with reference EA-PSI 8720-15 from EA-Elektro-Automatik.

In this thesis different measurements have been performed using this test configuration. A Tektronix current probe model TCP312 in conjunction with a Tektronix probe amplifier model TCPA300 was used for measuring the load currents. The current rating of the probe is 30 A DC, with a bandwidth of 100 MHz and a rise time of 3.5 ns. The gate voltage was measured using a differential probe model TA043 from Pico Technology with a bandwidth of 100 MHz. The gate current was measured indirectly, by means of capturing the voltage across the external gate resistance R_G^{EXT} using another differential probe model TA043 from Pico Technology. The drain-source voltage was measured using a high voltage differential probe model GDP-100 from GW Instek, with a bandwidth of 100 MHz. The oscilloscope used for capturing the waveforms was a Lecroy Wavesurfer 104MXs-B, with a bandwidth of 1 GHz and a rise time of 300 ps.

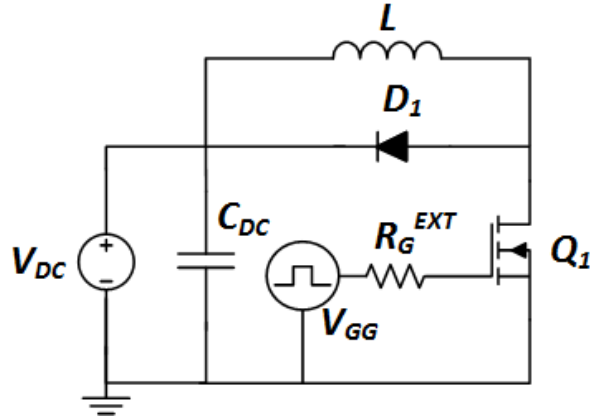
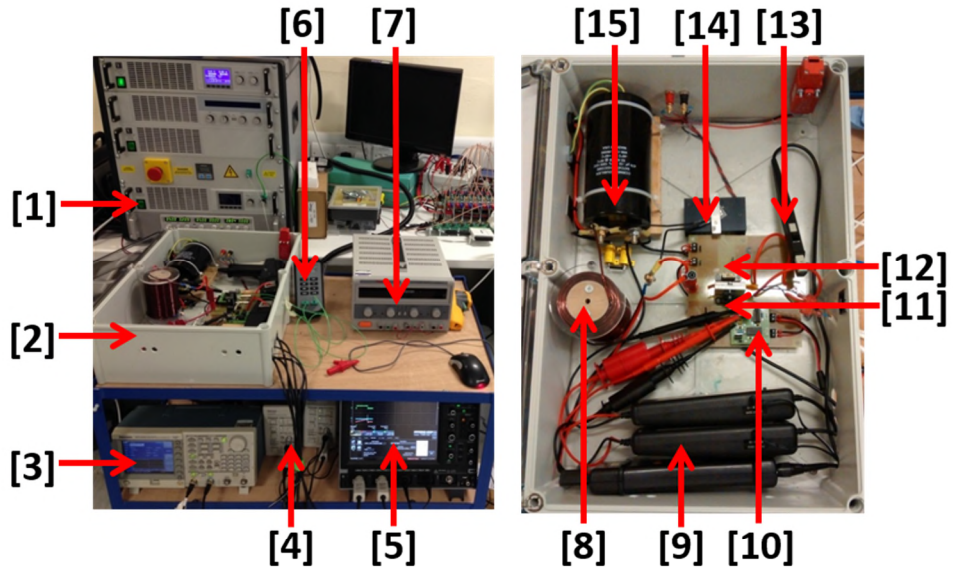


Figure 2.5 Schematic of a double pulse test circuit



[1] DC Power Supply, [2] Test Enclosure, [3] Function Generator, [4] Current Probe Amplifier, [5] Oscilloscope, [6] Thermometer, [7] DC Power Supply for the Heater, [8] Inductor, [9] Differential Voltage Probes, [10] Gate Driver, [11] Transistor Q_1 , [12] Heater, [13] Current Probe, [14] Freewheeling Diode D_1 , [15] DC Link Capacitor

Figure 2.6 Experimental setup of the double pulse test circuit

The circuit shown in Figure 2.5 is an ideal circuit, where the parasitic elements are not shown. Figure 2.7 presents a double pulse test setup where the main parasitic elements affecting the switching characteristics are shown.

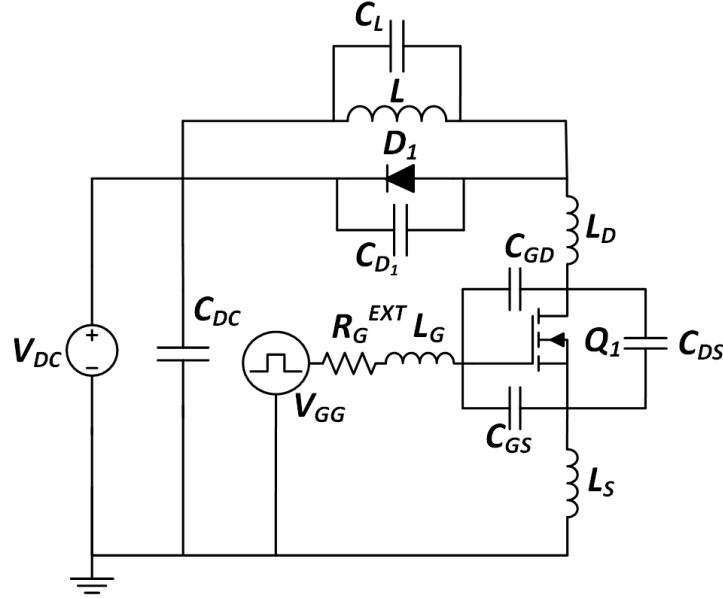


Figure 2.7 Schematic of a double pulse test circuit including the main parasitic elements

These parasitic elements include the parasitic capacitances of the device (in the case of a MOSFET: the gate-drain capacitance C_{GD} , the gate-source capacitance C_{GS} and the drain-source capacitance C_{DS}), the parasitic capacitance of the freewheeling diode and the inductor (identified C_L and C_{D1} in Figure 2.7) and parasitic inductances of the gate loop L_G , the common source L_S and the power loop L_D arising from the packaging and circuit interconnections [17, 19].

The charging and discharging of the parasitic capacitances define the turn-on and turn-off transient of the MOSFET, as it will be analysed in sections 2.3.4 and 2.3.5. [20, 21].

The parasitic gate loop inductance resonates with the input capacitance of the device causing oscillations in the gate voltage [17, 19]. The power loop inductance is the cause of ringing during switching transients. During turn-on, the responsible is the resonance between L_D and C_{par} (with $C_{par} = C_L + C_{D1}$) while during the turn-off transient the oscillations are determined by the resonance between L_D and the output capacitance of the MOSFET C_{OSS} (with $C_{OSS} = C_{DS} + C_{GD}$) [17, 19].

The parasitic capacitances of the freewheeling diode C_{D1} and the inductor C_L contribute to the current overshoot during turn-on, because of its charging during the turn-on transient [17, 22].

The impact of the source inductance is of particular interest from the point of view of the switching transients. The voltage across L_S reduces the effective gate-source voltage, slowing down the switching transients of the transistor [17]. The impact of the source inductance on the current switching rate and its temperature sensitivity will be analysed later on in chapter 3 of this thesis.

2.3 An overview of temperature sensitive electrical parameters for power devices

2.3.1 MOSFET on-state resistance

The on-state resistance of a power MOSFET has a well-known temperature dependency that is a function of channel resistance, the JFET resistance (for DMOS devices), the drift layer resistance and other series parasitic resistances like the terminal contact and substrate resistances [20].

The MOSFET on-state resistance has been used as a TSEP for the purpose of condition monitoring of SiC power MOSFETs in [23] and super-junction power MOSFETs in [24]. Measurements of the on-state resistance as a function of temperature have been made for 1200 V silicon MOSFETs and 900 V super-junction power MOSFETs (COOLMOS devices from Infineon). The measured resistance has been normalised respect to the value measured at 25 °C and it is shown in Figure 2.8, where a positive temperature coefficient (PTC) behaviour is clearly observed for both silicon devices using a gate-source voltage V_{GS} of 17 V. The on-state resistance was measured using the test setup for static TSEPs presented in section 2.2.

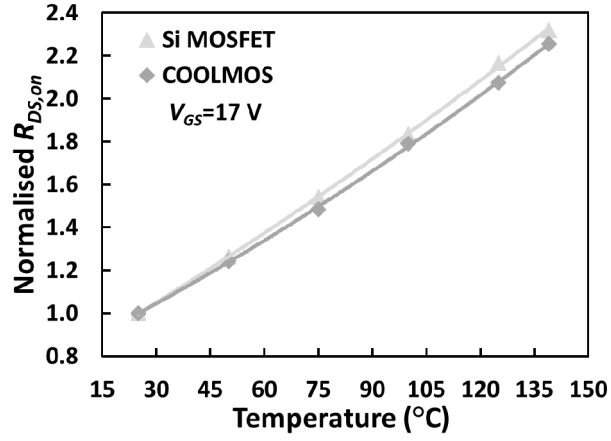


Figure 2.8 Normalised on-state resistance for different silicon MOSFET technologies

During self-heating pulses at high drain-source current I_{DS} values, the on-state drain-source voltage V_{DS} was captured and the results are presented in Figure 2.9. It is clearly observed how for the two different technologies the different power dissipation and different nominal on-state resistance cause different on-state voltages and different slopes, hence different junction temperatures. For the same load current the on-state voltage is considerable lower for the COOLMOS device, leading to a lower power dissipation, hence a reduced self-heating, as the measurements in Figure 2.9(a) show. Increasing the load current, as results in Figure 2.9(b) show, causes a higher power dissipation, hence the change in the on-state voltage for the heating pulse increases. This is an important consideration from the application point of view, as will be analysed later in this chapter.

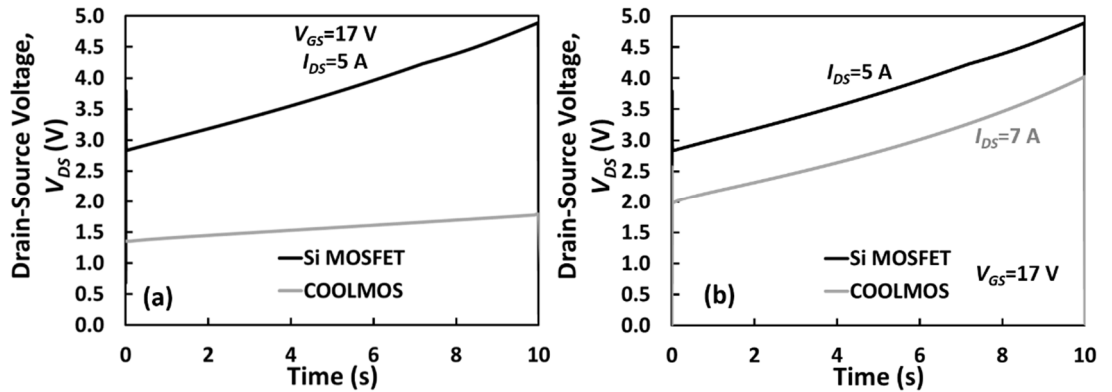


Figure 2.9 On-state voltage of a Si MOSFET and Si COOLMOS device during a self-heating pulse
(a) Same load current (b) Different load current

Since bond wire degradation and solder pad delamination increase the series resistance of the power MOSFET, the on-state resistance measured on-line can be used as a degradation indicator, as well as temperature indicator and it will be fundamental to decouple both effects [25].

The on-state resistance of SiC MOSFETs is analysed more in depth in chapter 4 of this thesis.

2.3.2 IGBT on-state collector to emitter voltage

The silicon IGBT is a hybrid between a BJT and a MOSFET. Structurally, it is similar to power MOSFETs with the exception that it sits on a p-substrate. It is essentially a MOS driven BJT whereby the drain of the MOSFET is connected to the base of an NPN BJT for an N-channel IGBT. It combines the advantages of the MOS gate structure from unipolar power MOSFETs with the conductivity modulation of bipolar devices. The IGBT uses conductivity modulation to achieve low on-state voltages and hence, low conduction losses. The conductivity modulation occurs when electrons from the channel of the MOS gate are injected into the voltage blocking n-drift region while holes are injected from the p+ collector into the drift region. Figure 2.10 shows the structural layout of an n-channel non-punch-through (NPT) IGBT and a n-channel punch-through (PT) IGBT.

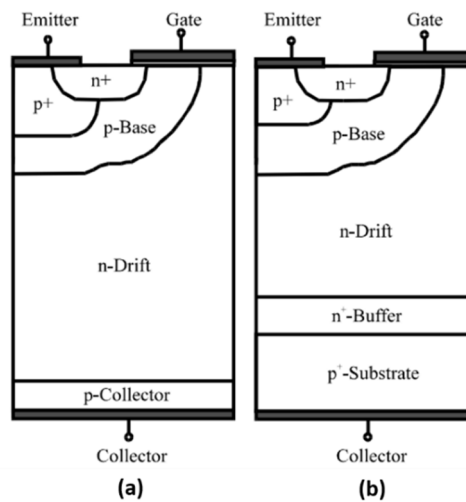


Figure 2.10 (a) Structural layout of a n-channel NPT-IGBT [26] (b) Structural layout of a n-channel PT-IGBT [26]

The primary difference between the NPT and the PT-IGBT is the presence of an n^+ buffer layer between the voltage blocking n -drift region and the p^+ collector. The purpose of this buffer layer in the punch-through IGBT is to increase the gradient of the electric field that is formed when the IGBT is blocking the off-state voltage since the gradient is proportional to the background doping. When IGBTs block voltage in the reverse mode, a depletion width is formed by the voltage blocking reverse biased PN junction and the maximum voltage the IGBT can block depends on the thickness and doping of this drift layer. However, by inserting the n^+ buffer layer, the rate of expansion of the depletion width is reduced since the gradient of the electric field is increased. As a result, PT-IGBTs will exhibit lower conduction losses compared to NPT-IGBTs [27].

In both IGBT structures shown in Figure 2.10, the gate has a planar structure. Using a trench gate the performance of the IGBT can be improved [20]. In the trench gate structure, the gate oxide and polysilicon gate are formed in a deep narrow trench below the chip surface [20, 28]. Both trench gate and planar gate structures are shown in Figure 2.11. With this gate structure the channel formed is vertical, whereas in the planar gate it is formed parallel to the surface of the chip, under the gate, as shown in Figure 2.11. The use of a trench gate provides a higher channel density resulting in a reduction of the channel resistance of the MOSFET portion of the IGBT and eliminates the JFET resistance [20, 28]. Moreover, the free carrier concentration is enhanced in the N -base region near the emitter [20].

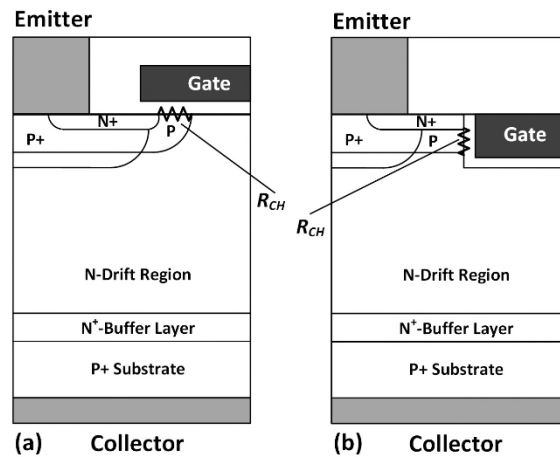


Figure 2.11 (a) PT IGBT with planar gate structure (b) PT IGBT with trench gate structure (Adapted from [29])

Basically, the on-state voltage drop of an IGBT can be modelled as the sum of the voltage drops of a MOSFET and a PiN diode and it is given by equation (2.1) [20], where k is the Boltzmann's constant, T the temperature, q the elementary charge, J_C the collector current density, W_N the width of the n-base region, D_a the diffusion coefficient, n_i the intrinsic carrier concentration, p the cell pitch, L_{CH} length of the channel, μ_{ni} channel mobility, C_{OX} the gate oxide capacitance density, V_G the gate voltage and V_{TH} the threshold voltage.

$$V_{on,IGBT} = \frac{2kT}{q} \ln \left[\frac{J_C W_N}{4q D_a n_i F \left(W_N / 2L_a \right)} \right] + \frac{p L_{CH} J_C}{\mu_{ni} C_{OX} (V_G - V_{TH})} \quad (2.1)$$

The first part of equation (2.1) is the forward voltage across a PiN diode and its temperature sensitivity will be analysed later in this chapter in section 2.3.3, however it is interesting to analyse some elements of the equation here. In equation (2.1), the function F in the denominator is a complex function that depends on the ratio of the drift layer thickness (W_N) to the ambipolar diffusion length (L_a), which is given by equation (2.2), where D_a is the ambipolar diffusion coefficient and τ_{HL} the carrier lifetime at high injection.

$$L_a = \sqrt{D_a \tau_{HL}} \quad (2.2)$$

When the IGBT is in the on-state, the voltage drop increases with temperature as a result of mobility degradation in the channel and the bulk. However, at low current levels, when there is low level minority carrier injection into the drift region, the on-state voltage has a negative temperature coefficient. This is due to the reduction of the junction voltage at the p+ collector/n-drift PN junction due to an increase in the intrinsic carrier concentration, as well as the increase in the minority carrier lifetime. Hence, the on-state voltage of IGBTs has a Zero Temperature Coefficient (ZTC) point at which the temperature coefficient of the on-state voltage switches from being negative at low current levels to positive at high current levels. For a better understanding of the temperature coefficients, the crossover point (ZTC) and the NTC/PTC areas of the output characteristics of an IGBT are shown in Figure 2.12.

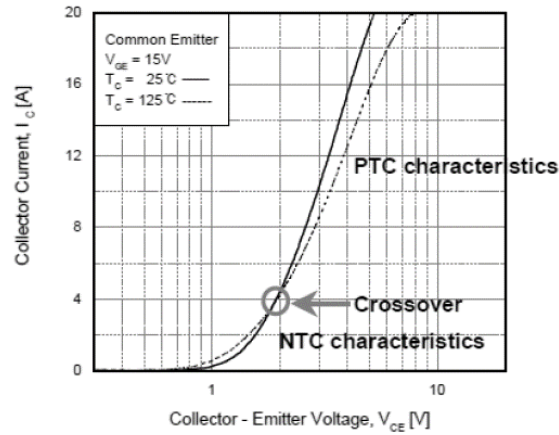


Figure 2.12: Output characteristics of an IGBT, from [30]

Depending on the IGBT structure and manufacturing process, the contributions to the on-state voltage of the diode and MOSFET elements are different, resulting in different ZTC points and different temperature coefficients [31].

Measurements have been performed on 1200 V silicon IGBTs from Infineon with datasheet reference IGW15T120 and a current rating of 15 A at 100 °C. Figure 2.13 shows the on-state voltage as a function of temperature with a collector current of 25 and 50 mA, which is clearly below the ZTC. The gate voltage applied to turn-on the IGBT was $V_{GE}=17$ V.

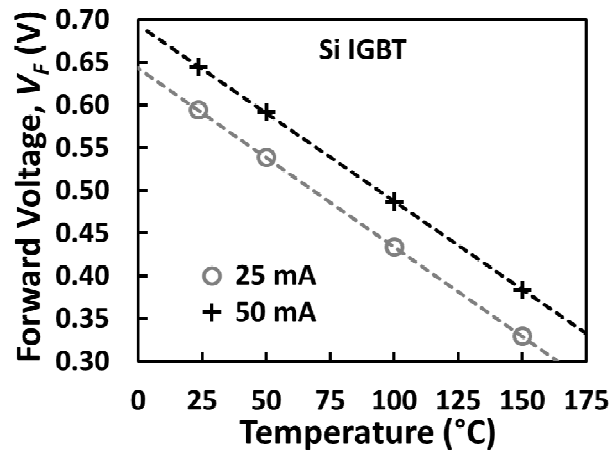


Figure 2.13: On-state voltage of a 1200V/15 A IGBT as a function of temperature at low currents

The voltage during self-heating at high currents has also been captured and it is shown in Figure 2.14 where the existence of a ZTC is clearly observable.

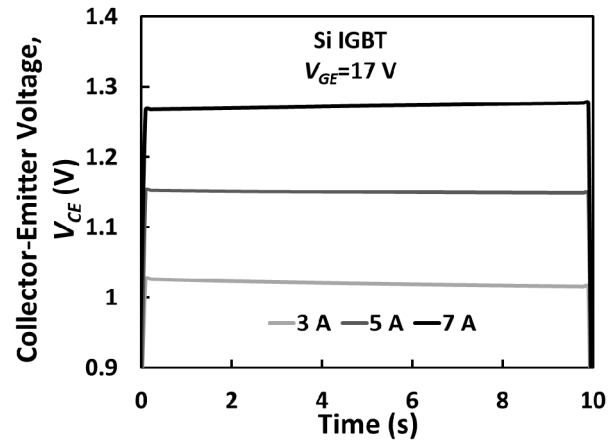


Figure 2.14 On-state voltage of the selected IGBT during self-heating at different current levels

The on-state voltage at low currents, where the self-heating can be considered negligible is a good indicator of the junction temperature and it is widely used as an indicator of degradation of the thermal resistance during power cycling tests, for example in [32]. Advanced equipment can be used for capturing the transient thermal impedance during the cooling transient and evaluate the degradation of the packaging [33] and the on-state voltage at high current as TSEP has also been used in [34].

2.3.3 Diode junction forward voltage

Schottky diodes are rectifying devices comprised of a metal contact directly on a semiconductor. Hence, unlike the PN junction characteristic in bipolar devices, the Schottky rectifying contact is unipolar in the sense that current flow is due to the drift of the majority carrier and not the diffusion of a minority carrier. The in-built junction voltage in a Schottky rectifier is formed by the Schottky barrier height. The Schottky barrier height, in turn, is dependent on the metal-semiconductor work-function difference. Here, the work-function in the metal is defined as the energy required to move an electron from the Fermi level of the metal to vacuum level while the work-function of the semiconductor is similarly defined as the energy required to move an electron from the Fermi-level of the semiconductor to vacuum level. Figure 2.15 shows the energy band-diagram of a metal-semiconductor contact before and after intimate contact is made between the metal and the semiconductor.

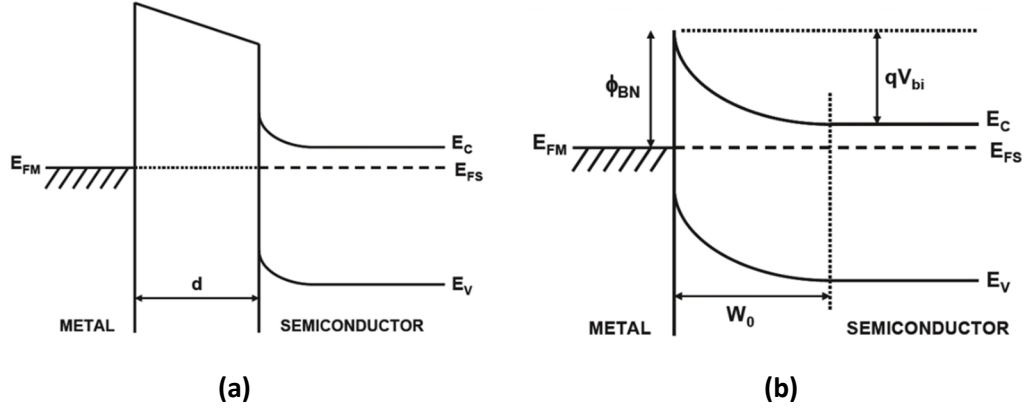


Figure 2.15 Energy band-diagram of a metal semiconductor contact, from [20] (a) Before intimate contact, (b) After intimate contact

The difference between the work-function of the metal and the work-function of the semiconductor is called the contact potential (V_C). This contact potential is related to the Schottky barrier potential according to equation (2.3), with E_{FS} the Fermi level position in the semiconductor, E_{FM} the Fermi level in the metal, ϕ_M the work function of the metal, ϕ_S the work function for the semiconductor, χ_S electron affinity for the semiconductor and E_C the bottom of the conduction band in the semiconductor.

$$qV_C = (E_{FS} - E_{FM}) = \phi_M - \phi_S = \phi_M - (\chi_S + E_C - E_{FS}) \quad (2.3)$$

This contact potential forms a depletion width within the semiconductor when intimate contact is made between the metal and the semiconductor. This depletion width arises from the fact that excess electrons from the n-doped semiconductor will diffuse across the Schottky contact into the metal, thereby depleting the semiconductor at the contact interface. When the contact voltage falls across the semiconductor and depletes the surface, it is referred to as the in-built voltage (V_{bi}) which relates to the Schottky barrier height (ϕ_{BN}) according to equation (2.4).

$$\phi_{BN} = qV_{bi} + (E_C - E_{FS}) \quad (2.4)$$

Under forward conduction mode, electrons are injected from the semiconductor into the metal whereas holes go from the metal into the semiconductor. The forward current is comprised of thermionic emission current (thermal excitation of electrons across the barrier height), tunnelling current (due to quantum mechanical tunnelling of

electrons through the Schottky barrier) and recombination currents due to minority carrier diffusion. For high voltage Schottky rectifiers used in high power applications, the forward current is dominated by thermionic emission of electrons across the Schottky barrier from the semiconductor. The equation governing field emission theory in Schottky contacts is given by equation (2.5), where J_F is the forward current density, A is the Richardson's constant, ϕ_{BN} the Schottky barrier height, T is the temperature, k the Boltzmann's constant and V_F the forward voltage.

$$J_F = AT^2 e^{-\frac{q\phi_{BN}}{kT}} \left(e^{\frac{qV_F}{kT}} - 1 \right) \quad (2.5)$$

For high voltage rectifiers with large forward voltages, equation (2.5) can be re-written as

$$J_F = AT^2 e^{-\frac{q\phi_{BN}}{kT}} e^{\frac{qV_F}{kT}} = J_S e^{\frac{qV_F}{kT}} \quad (2.6)$$

In equation (2.6) above, J_S is the saturation current density which depends on the Richardson's constant A and the Schottky barrier height ϕ_{BN} . Hence, the forward voltage V_F in Schottky rectifiers can be expressed as

$$V_F = \frac{kT}{q} \ln \left(\frac{J_F}{J_S} \right) \quad (2.7)$$

To show the impact of temperature on the forward voltage, equation (2.7) can be re-written as

$$V_F = \phi_{BN} + \frac{kT}{q} \ln \left(\frac{J_F}{AT^2} \right) \quad (2.8)$$

It can be seen from equation (2.8) that temperature appears in the denominator of the logarithm term, hence, the forward voltage decreases with temperature. However, this is true only at low currents. As the current is increased, the voltage drop across the series parasitic resistances of the Schottky diode dominates the forward voltage, hence, the total on-state voltage increases with temperature at high currents. The total forward voltage

across the Schottky rectifier $V_{F,total}$ is given by the sum of the forward junction across the rectifying junction as well as the voltage drop across the voltage blocking semiconductor layer $R_{D,sp}$, the voltage drop across the semiconductor substrate R_{SUB} as well as the contact resistances R_{CONT} , as given by equations (2.9) and (2.10).

$$V_{F,total} = V_F + V_R = \frac{kT}{q} \ln \left(\frac{J_F}{J_s} \right) + J_F \cdot R_{S,sp} \quad (2.9)$$

$$R_{S,sp} = R_{D,sp} + R_{SUB} + R_{CONT} \quad (2.10)$$

Hence, at low forward currents, the forward voltage has a negative temperature coefficient i.e. it decreases with increasing temperature due to increased thermionic emission of electrons across the Schottky contact barrier height. However, at high current densities, the increased voltage drop across the series parasitic resistance causes the forward voltage to have a positive temperature coefficient. This is due to increased phonon scattering reducing the carrier scattering relaxation time and hence, the carrier mobility which the result of increasing the resistivity of the semiconductor.

Figure 2.16 shows measurements of the temperature dependency of the forward voltages in SiC Schottky diodes at high currents whereas Figure 2.17 shows the same characteristics at low forward currents. The forward voltage at high currents was captured during self-heating of the device, whereas the forward voltage as low currents was captured heating the device externally. The device evaluated is a 600 V/4 A SiC Schottky from Cree/Wolfspeed with datasheet reference C3D02060A.

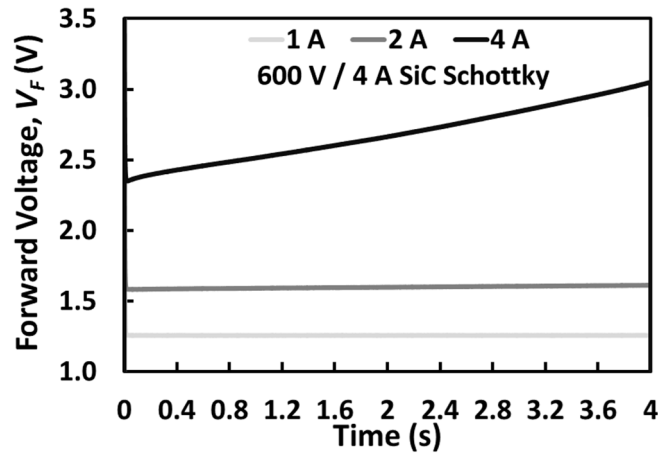


Figure 2.16 Forward voltage during self-heating of a 600 V/4 A SiC Schottky

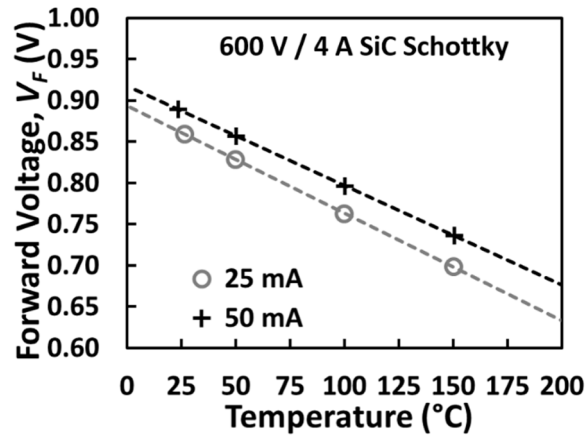


Figure 2.17 Forward voltage at low currents of a 600 V/4 A SiC Schottky

The current at which the on-state voltage does not change with temperature is called the zero-temperature coefficient (ZTC) current and is a very important consideration in the paralleling and series connection of Schottky power diodes.

Unlike Schottky diodes, PiN diodes are bipolar devices because current transport is due to the diffusion of minority carriers as opposed to the drift of majority carriers in Schottky diodes. PiN diodes are comprised of a low doped n-drift region sandwiched between a highly doped p+ anode and a highly doped n+ cathode. The reverse voltage in a PiN diode is blocked by a PN junction formed between the p+ anode and the low doped n-drift region. During forward conduction mode, the current transport mechanisms are the recombination currents in the space charge layer, diffusion of minority carriers injected into the drift region and conductivity modulation from electrons and holes in the drift region. Figure 2.18(a) shows a one-dimensional cross-section of a PiN diode together with the electric field formed across the drift region while Figure 2.18(b) shows the internal carrier density profile across the PiN diode.

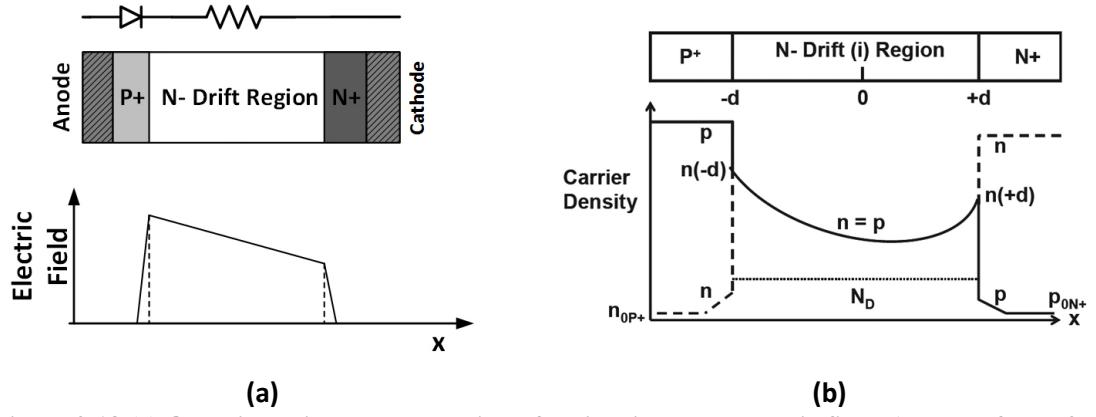


Figure 2.18 (a) One-dimensional cross-section of a PiN diode and electric field. Adapted from [35]
 (b) Carrier density profile across a PiN diode, from [20]

The forward voltage of the PiN diode is comprised of the sum of the junction voltage between the p+ anode/n-drift junction, the n- drift/n+ cathode junction and the voltage drop across the drift layer. The junction voltages (V_{N+} and V_{P+}) can be expressed as

$$V_{P+} = \frac{kT}{q} \ln \left[\frac{p(-d)N_D}{n_i^2} \right] \quad (2.11)$$

$$V_{N+} = \frac{kT}{q} \ln \left[\frac{n(+d)}{N_D} \right] \quad (2.12)$$

where k is the Boltzmann's constant, T is temperature, q is the elementary charge, d is half the thickness of the drift region, $p(-d)$ concentration for holes at $-d$, $n(+d)$ the concentration for electrons at $+d$, n_i the intrinsic carrier concentration and N_D is background doping concentration.

The voltage drop across both junctions, assuming charge neutrality is

$$V_{P+} + V_{N+} = \frac{kT}{q} \ln \left[\frac{n(-d)n(+d)}{n_i^2} \right] \quad (2.13)$$

The voltage drop across a drift layer of total thickness w_d is given equation (2.14), where μ_n is the electron mobility, μ_p is the hole mobility and τ_{HL} the carrier lifetime at high injection.

$$V_{drift} = \frac{w_d^2}{(\mu_n + \mu_p)\tau_{HL}} \quad (2.14)$$

The temperature dependency of the PiN diode forward voltage is determined by the temperature dependencies of the different elements. At low current, the junction voltages are the main contributors to the total on-state voltage. Because the junction voltages (V_{N+} and V_{P+}) are inversely related to the intrinsic carrier concentration n_i , and the intrinsic carrier concentration increases with temperature, the junction voltages reduce with temperature. The temperature dependency of the intrinsic carrier concentration is given by equation (2.15), where n is the density of n-type carriers, p is the density of p-type carriers, N_C is the density of states at the bottom of the conduction band, N_V is the density of states at the top of the valence band and E_G the bandgap energy.

$$n_i = \sqrt{np} = \sqrt{N_C N_V} e^{-E_G/2kT} \quad (2.15)$$

Thermal excitation of the crystal lattice induces free carriers with sufficient thermal energy to cross the bandgap thereby increasing the intrinsic carrier concentration. Semiconductors with a wider bandgap (e.g. SiC with 3.23 eV and GaN with 3.4 eV) will therefore exhibit reduced free carrier concentration, since for any given temperature less carriers will attain the sufficient energy for carrier generation across the bands. As a result of the positive temperature coefficient of the intrinsic carrier concentration, the junction voltages and the total forward voltage reduce with increasing temperature at low current densities. However, as the current density increases, the voltage drop across the drift region, modelled by equation (2.14), dominates the total voltage drop.

Analysing equation (2.14), the temperature dependency is given by both the carrier mobility (μ_n and μ_p) and the carrier lifetime (τ_{HL}). The mobility decreases with temperature, leading to an increase of V_{drift} and the carrier lifetime increases with temperature, causing a reduction of V_{drift} . Both effects oppose and what will determine the temperature coefficient of V_{drift} is the technology used for the recombination centres [31].

As is the case with other devices, the ZTC point in the forward characteristics of the PiN diode is defined as the point where the opposing effects of reducing junction voltage with temperature and increasing drift layer voltage drop with temperature are perfectly counterbalanced. This can be identified in the forward voltage characteristics measured at different temperatures. PiN diodes, however, exhibit a higher ZTC point in

current compared to Schottky diodes. This is due to the fact that it is a bipolar device with minority carriers hence, carrier lifetime and junction voltages play important roles in the temperature characteristics, with the technology used for fabricating the diode playing a fundamental role in the value of the ZTC [31]. The higher ZTC of the PiN diodes makes them less electrothermally stable under parallel connections compared with Schottky diodes. If parallel diodes are conducting a current below the ZTC point, then hotter diode will conduct more current because of the lower forward voltage. This causes a positive feedback loop between current and temperature which can lead to thermal runaway since the hotter diode continues to demand more current while the cooler diode demands less current [36]. This is a crucial disadvantage of PiN diodes in high power applications where paralleling is required for high current conduction capability.

As in the case of IGBTs, the on-state voltage at low currents of both PiN and Schottky diodes, where the self-heating is considered negligible, it is a good indicator of the junction temperature and it can be used for monitoring the degradation of the transient thermal impedance. This TSEP requires the calibration of the forward voltage for the selected sensing current, as in the case of IGBTs and Schottky diodes. Figure 2.19 shows the forward voltage temperature sensitivity measured from a 600V/4A PiN diode from International Rectifier with datasheet reference HFA04TB60.

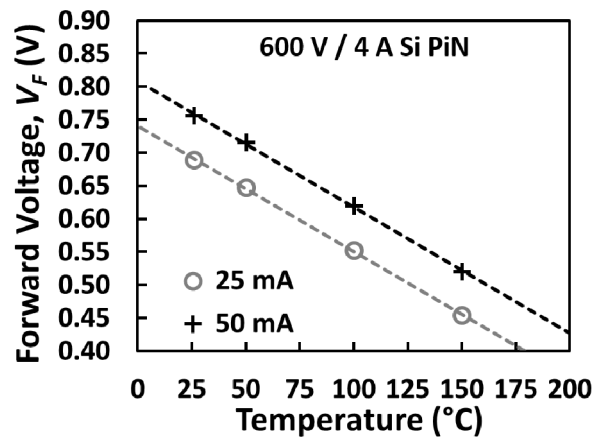


Figure 2.19 Forward voltage at low currents of a 600 V/4 A Si PiN diode HFA04TB60

The parasitic body diode of a MOSFET is also a PN junction which could also be used for temperature sensing and thermal resistance monitoring [37-39].

2.3.4 MOSFET/IGBT threshold voltage and turn-on delays

The threshold voltage of the power MOSFET is simply defined as the minimum voltage of the gate terminal that is required to uniformly invert the channel from p-type to n-type. This definition holds for n-type MOSFETs, which are the dominant FET devices used in low voltage power electronics. This derivation of the equation for the threshold voltage and the understanding of its temperature sensitivity requires a brief revision of band theory in power devices.

IGBTs and power MOSFETs have MOS gate contacts comprising of a metal (degenerately doped n-type polysilicon), an oxide (a thermally grown layer of silicon dioxide) and a semiconductor (a p-type silicon or SiC layer that is inverted to form a channel). When a voltage is applied at the gate of the MOSFET, the channel beneath the gate can go into accumulation, depletion or inversion. If a negative voltage is applied, the channel is in accumulation with majority carriers since the positively charged channel dopants are attracted by the negative direction of the electric field. As the gate voltage becomes more positive, the channel goes into depletion since the positively charged majority carriers are repelled by the positive electric field across the channel. The minimum gate voltage at which the p-channel becomes inverted is the threshold voltage. This is also defined as the voltage at which the electron concentration in the channel of the MOSFET is at least equal to the p-type background doping. The threshold voltage will be the sum of the flatband voltage (due to the metal semiconductor work-function difference), the voltage drop across the gate oxide and the surface potential of the semiconductor. The threshold voltage will depend on the thickness of the gate dielectric and the p-type doping of the channel according to the equation below, where V_{FB} is the flatband voltage, ϕ_s the surface potential of the semiconductor, N_A is the doping concentration, n_i is the intrinsic carrier concentration, ϵ_{Si} the dielectric constant of silicon and C_{OX} the gate oxide capacitance density.

$$V_{TH} = V_{FB} + \phi_s + \frac{\sqrt{qN_A\epsilon_{Si}2\phi_s}}{C_{OX}} \quad (2.16)$$

with

$$\phi_s = 2 \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) \quad (2.17)$$

Since the threshold voltage is inversely related to the intrinsic carrier concentration, then it will reduce with increasing temperature since the intrinsic carrier concentration exhibits a positive temperature coefficient. In other words, as the thermal energy in the crystal lattice of the semiconductor is increased, there is sufficient energy for carrier generation across the bandgap, hence, less voltage is required for inverting the channel. MOSFETs and IGBTs as a result have threshold voltages that reduce with increasing temperature. In SiC power MOSFETs, this effect is less pronounced since the rate of carrier generation across the bandgap is smaller as a result of the 3.3 eV bandgap compared to the 1.12 eV bandgap in silicon devices.

The threshold voltage can therefore be used as a TSEP in MOSFETs and IGBTs since the temperature dependency of the threshold voltage can be calibrated beforehand. A few researchers have attempted to use the threshold voltage as a TSEP for on-line condition monitoring in silicon devices [37, 40], however, difficulties persist due to the measurement resolution required for extracting the threshold on-line using dynamic measurements. The impact of a lower threshold voltage on the turn-on transient can be evaluated using the current transient, as the time where the current starts to rise (t_{TH}) is determined by the threshold voltage according to

$$t_{TH} = (R_G)C_{ISS} \ln\left(\frac{V_{GG}}{V_{GG} - V_{TH}}\right) \quad (2.18)$$

where R_G is the total gate resistance comprising the external gate resistance and the internal gate resistance of the device, C_{ISS} is the input capacitance, V_{GG} the supply voltage of the gate driver. The time t_{TH} is also a temperature sensitive parameter [41].

Figure 2.20 shows the impact of the lower threshold voltages on the turn-on transient of the turn-on current as a function of temperature for a silicon MOSFET, whereas Figure 2.21 shows an IGBT and Figure 2.22 shows for a COOLMOS device. It is clearly observed how the lower threshold voltage causes the device to turn on sooner in time, i.e. a lower t_{TH} for all the devices evaluated.

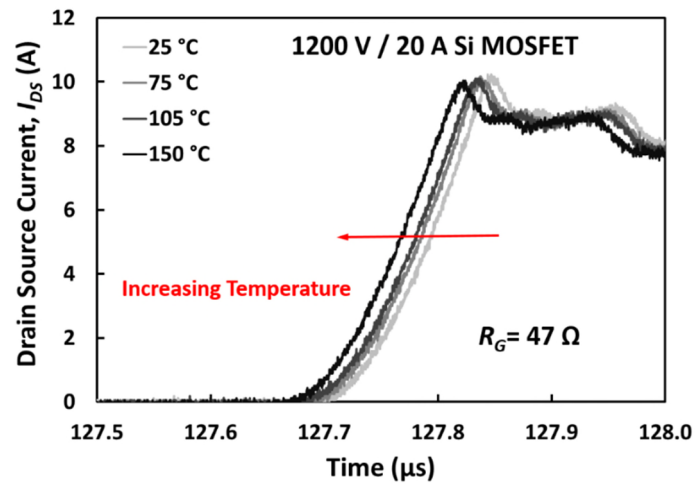


Figure 2.20 Drain-source current turn-on transient at different temperatures of a Si MOSFET

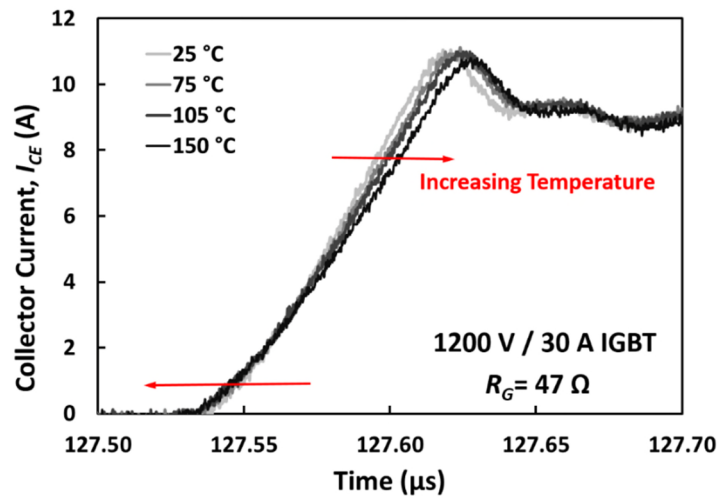


Figure 2.21 Collector-emitter current turn-on transient at different temperatures of a Si IGBT

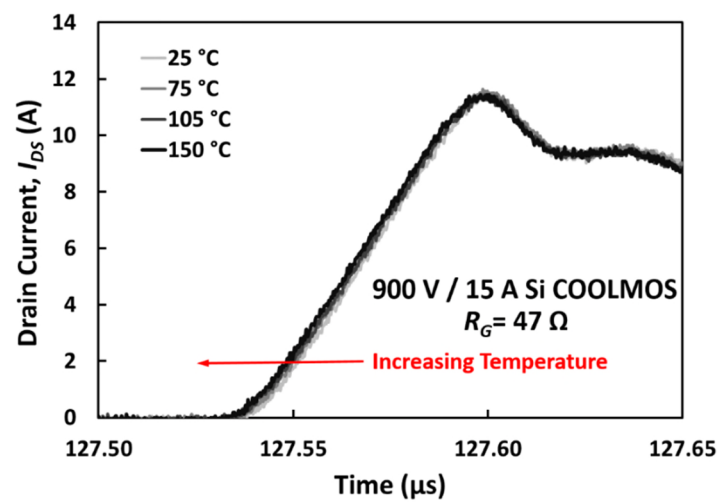


Figure 2.22 Drain-source current turn-on transient at different temperatures of a Si COOLMOS

In the case of the IGBT the switching rate of the current it is observed how the switching rate of the current is affected by temperature, as the results in Figure 2.21 indicate. The impact of temperature of the switching rate as a function of technology will be evaluated in chapter 3, including SiC MOSFETs.

2.3.5 *Miller plateau discharge – Turn-off delay*

The Miller plateau is a feature in the gate transient characteristics of power MOSFETs and IGBTs. Since the MOS gate terminals of power MOSFETs and IGBTs contain inherent parasitic capacitances that must be charged during turn-on and discharged during turn-off, the Miller plateau arises from the charging of these capacitors. Specifically, there are two parasitic capacitances related to the MOS gate namely, the gate-source capacitance and the gate-drain capacitance, otherwise known as the Miller capacitance. The gate-source (gate-emitter for IGBTs) capacitance arises from the overlap between the gate terminal and the n-doped source terminal whereas the gate-drain (gate-collector for IGBTs) capacitance arises from the overlap between the gate and n-drift region. Both capacitances are dependent on the oxide thickness and overlap area. However, the gate-drain capacitance is a series combination of the oxide capacitance and the depletion capacitance arising from the space charge layer that is formed when the drift layer is blocking the DC voltage. Because the Miller capacitance is formed by the oxide capacitance as well as a voltage dependent depletion capacitance, it is a non-linear capacitance that decreases as the drain (collector for IGBT) voltage increases. This is due to the fact that the depletion width increases with the drain (collector for IGBT) voltage. Figure 2.23 shows the cross-section of a power MOSFET and the electrical schematic circuit diagram showing the parasitic capacitances (C_{GS} , C_{GD} and C_{DS}), parasitic body diode and main parasitic resistive elements (channel resistance R_{CH} and n-layer resistance R_{EPI}).

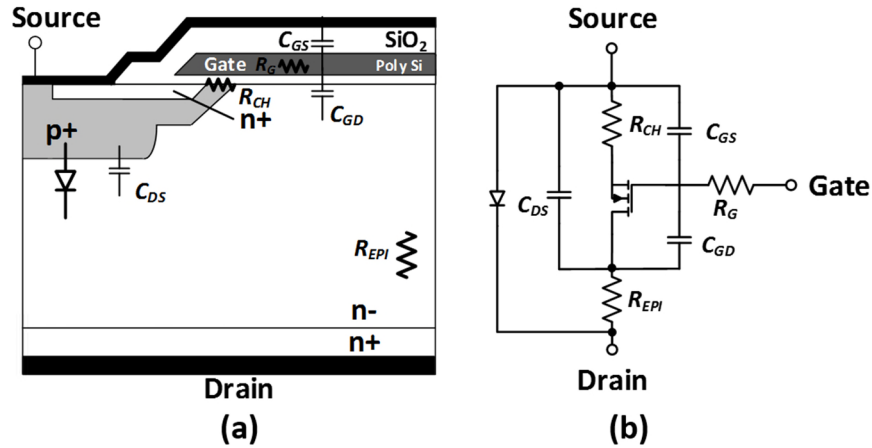


Figure 2.23 (a) Cross-section of a MOSFET (b) Electrical schematic of a MOSFET showing the parasitic capacitances (Adapted from [31])

Figure 2.24 shows a sketch of the gate-source voltage, drain-source current and drain-source voltage transients of a MOSFET (or an IGBT). As the gate voltage is increased between time t_0 and t_1 , the gate-source capacitance is charged at a rate that depends on the gate resistance and the gate-source (emitter for IGBT) capacitance. At time t_1 , when the threshold voltage is reached, the MOSFET (IGBT) channel conducts current which rises until the load current value at t_2 . At this point, the gate-source (emitter) capacitor stops charging as the gate current is diverted to the gate-drain (collector) capacitance. The charging of the Miller capacitance precipitates the fall of the drain (collector) voltage from the off-state blocking value to the on-state value. For the duration of the t. At the point when the voltage transient ends, the Miller capacitance stops charging and the gate current is re-directed to the gate-source capacitance. This occurs at time t_3 in Figure 2.24.

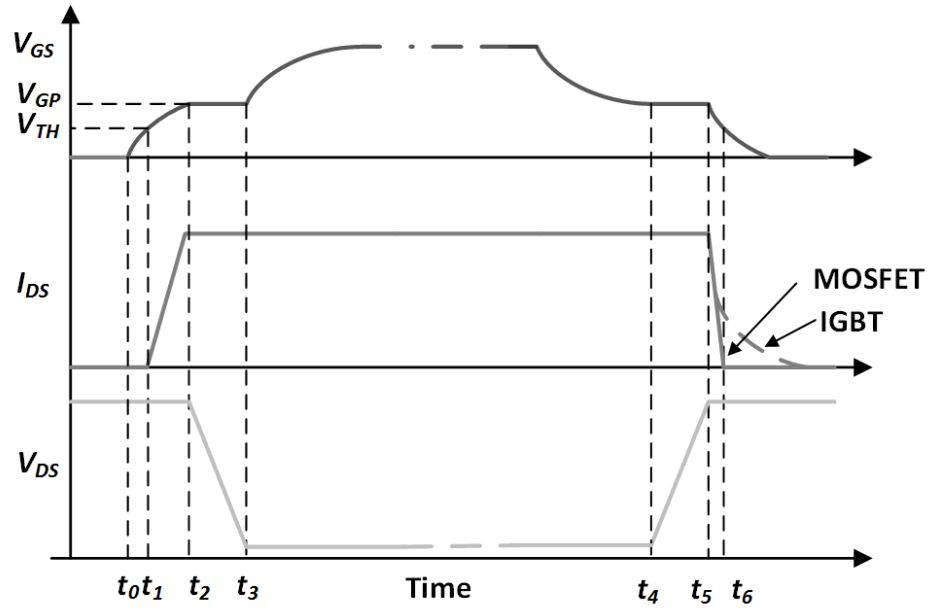


Figure 2.24 Idealised waveforms during the turn-on and turn-off transients of a MOSFET
(Adapted from [21])

During the turn-off transient, the process occurs in the reverse direction, as it is observed in Figure 2.24. The gate voltage decreases exponentially until it reaches the plateau voltage V_{GP} at t_4 . During the plateau time, the load current and the gate voltage remain constant. The gate-drain (gate-collector) capacitance is discharged and the drain (emitter) voltage starts to increase. Once the plateau finishes and the drain voltage has reached the off-state value, at the instant t_5 , the gate capacitance continues to discharge and the load current decreases until the threshold voltage is reached at t_6 . Once the current is zero, the gate voltage continues to decrease exponentially until it is zero. In the case of the IGBT, the transients are similar but there is a characteristic tail current caused by recombination of the charge carriers remaining in the device [31]).

The Miller plateau voltage V_{GP} is shown in Figure 2.24 and is defined as the gate voltage plateau level during the drain (collector) transient when the Miller capacitance is charged during turn-on and discharged during turn-off.

The temperature dependency of the Miller plateau is due to the drain (collector) voltage transient temperature dependency. The time duration of the plateau voltage has been identified as a TSEP in silicon IGBTs in [42]. Figure 2.25 shows measurements of IGBT gate transients at different temperatures where the temperature sensitivity of the

Miller plateau can be observed, while Figure 2.26 shows the impact of temperature on the turn-off transient of the collector-emitter voltage, which was evaluated as TSEP in [43].

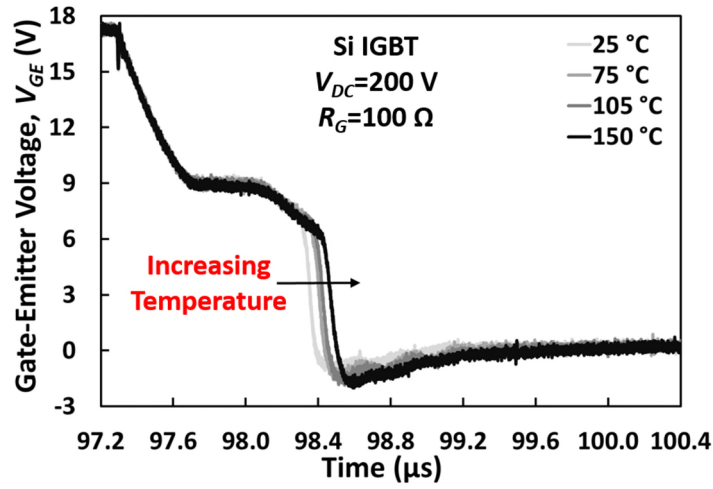


Figure 2.25 Gate-Emitter voltage during turn-off of a Si IGBT at different temperatures

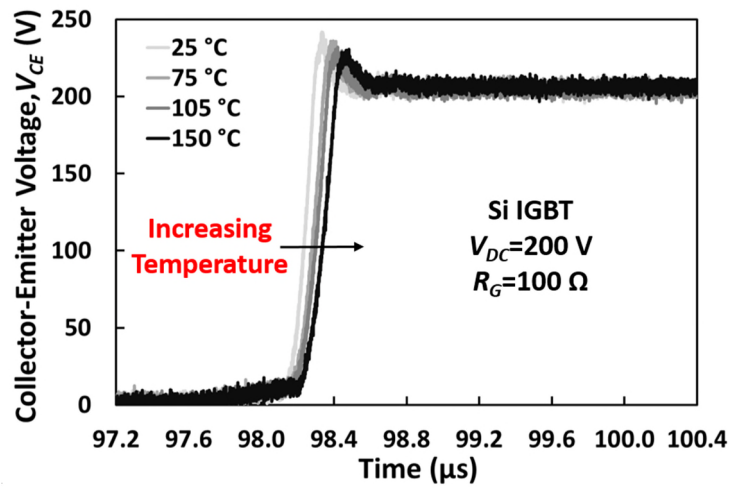


Figure 2.26 Collector-Emitter voltage during turn-off of a Si IGBT at different temperatures

Slowing down the device, by means of increasing the gate resistance increases the temperature sensitivity, as it can be observed in Figure 2.27.

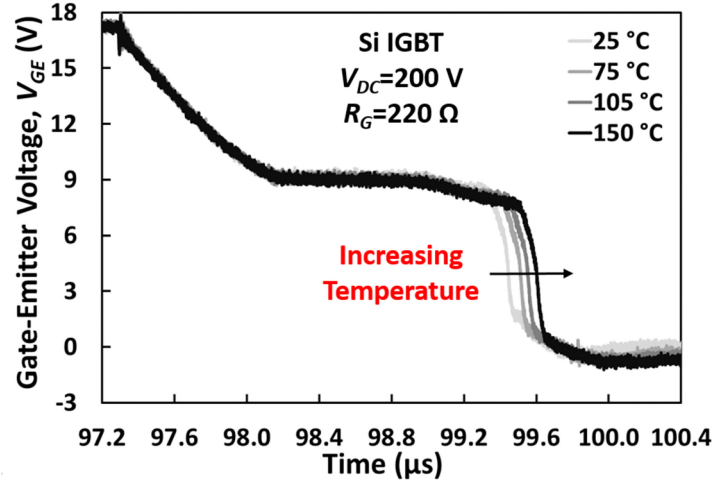


Figure 2.27 Impact of slowing down the turn-off of a Si IGBT on the gate-emitter voltage transient

In the case of silicon MOSFETs and IGBTs the delay between the instant when the gate is triggered and the instant when the current starts falling to zero can also be used as a TSEP. It has been evaluated for silicon IGBTs in [44], where the voltage across the parasitic emitter inductance was used as sensor. In the case of the IGBT, the impact of temperature is also observed in the tail current, as the results in Figure 2.28 show.

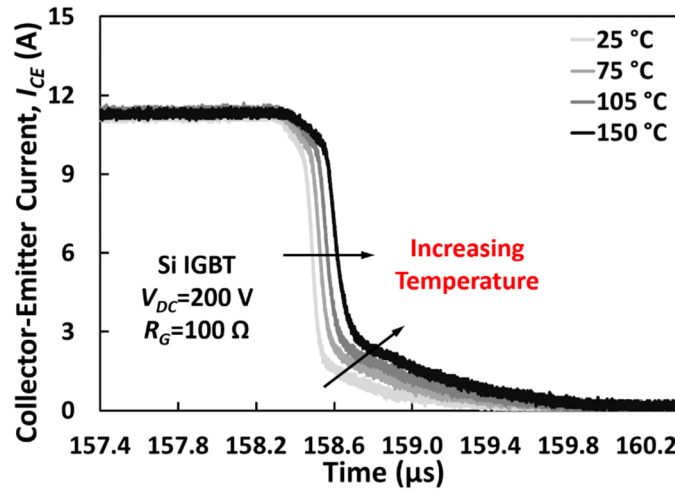


Figure 2.28 Collector-Emitter current during turn-off of a Si IGBT at different temperatures

2.3.6 PiN diode reverse recovery

As was described earlier, the PiN diode is a bipolar device based on minority carrier diffusion and conductivity modulation in the voltage blocking drift region. As a result, it is able to maintain low conduction losses, since a high density carrier plasma is

formed during conductivity modulation. However, as the diode is turned OFF and starts to block the DC voltage, the removal of these minority carriers results in reverse recovery. The typical reverse recovery characteristics of a PiN diodes is shown in Figure 2.29 which applies to a diode commutating current with a complementing transistor driving an inductive load. As the diode is turned off, the current commutation rate (dI_F/dt) will depend on the transistor commutating current away from the diode since the diode is a passive device. In Figure 2.29, between t_0 and t_1 , the current through the diode ramps down as the current through the complementing transistor ramps up. At time t_1 , due to the stored charge in the diode, the current goes negative and continues until the voltage initially across the MOSFET starts to build up across the diode. At the time the polarity across the diode changes from forward biased to reverse biased, a depletion width forms at the anode PN junction thereby cutting off the supply of minority carriers to the external circuit. As a result, the remaining carriers in the drift region of the diode can no longer be extracted and therefore have to recombine. The rate at which these minority carriers recombine will depend on the lifetime of the minority carriers.

Since, carrier lifetime increases with temperature, the total stored charge in the drift region of the diode increases with temperature. Hence, the peak reverse recovery current is a TSEP. The reverse recovery current in PiN diodes has been used as a TSEP, as detailed in [16]. The peak reverse recovery current I_{RRM} will depend not only on temperature but also on the current commutation rate in the circuit and the parasitic inductance in the path of current flow. If the latter parameters are well characterised, then the temperature of the diode can be inferred from the peak reverse recovery current.

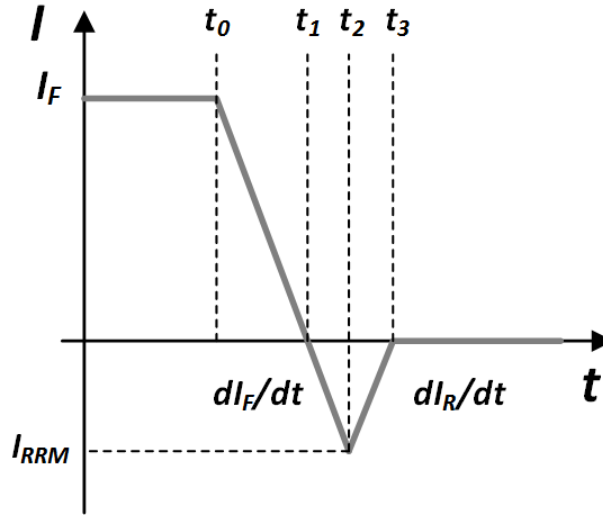


Figure 2.29 Turn-off transient of a PiN diode

Measurements have been done on a 600 V silicon PiN diode from International Rectifier with a current rating of 15 A at 140 °C with datasheet reference 15ETH06 at different temperatures. Figure 2.30 shows the results. For the selected diode, in addition to the increase of maximum reverse recovery current (I_{RRM}), Figure 2.30 shows an increase of the reverse recovery switching rate dependent on the diode temperature dI_R/dt [45]. The complementary MOSFET is driven with a gate resistance R_G^{EXT} of 150 Ω

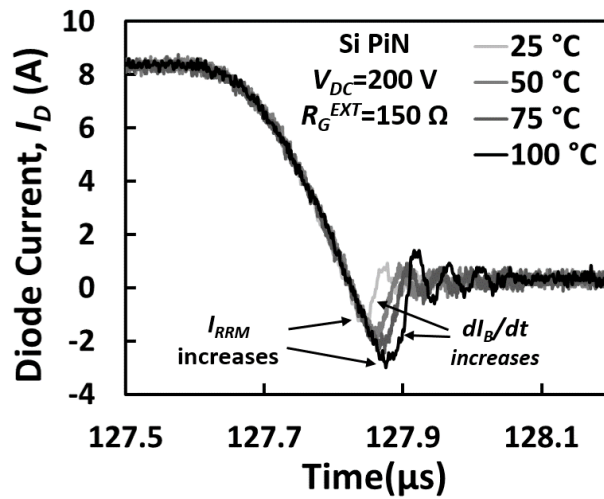


Figure 2.30 Impact of temperature on the reverse recovery of the PiN diode during the turn-off transient

The impact of the switching rate of the complementary MOSFET can be observed in Figure 2.31.

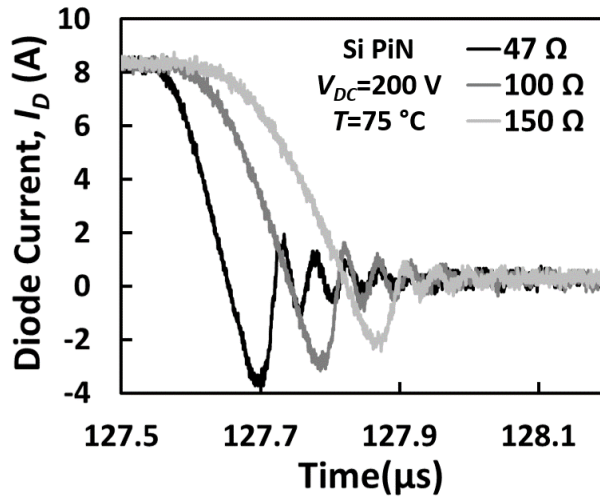


Figure 2.31 Impact of the switching rate of the complementary MOSFET on the reverse recovery of the PiN diode during the turn-off transient

2.4 Electrothermal considerations for power cycling in silicon and silicon carbide power devices

In the application voltage range between 600 V and 1700 V, there is intense competition between silicon bipolar and silicon carbide unipolar devices. Silicon bipolar diodes use conductivity modulation to reduce conduction losses while SiC unipolar devices use high current/voltage commutation rates to reduce the switching losses. The absence of minority carriers in SiC unipolar devices means that switching rate is limited by the charging/discharging of junction capacitances whereas in bipolar devices with minority carriers, minority carrier lifetime is a limiting factor in switching rate. As a result, depending on the application, either technology may be preferred. However, one of the main challenges impeding SiC penetration into different sectors is the relatively unknown reliability of SiC devices. As a result of the wide bandgap and high critical electric field, SiC unipolar devices are geometrically smaller and as a result have smaller parasitic capacitances. The fact that SiC die are smaller means that there will be different stresses generated in the die/solder interface as it undergoes power cycling. This section of the thesis will investigate the power cycling performance of SiC power devices under constant current stress tests. Power cycling and thermal impedance characterisation

techniques mentioned earlier have been used to electrothermally characterise SiC Schottky diodes and silicon PiN diodes.

2.4.1 Test configuration and calibration of TSEPs

A widely used method for power cycling is the use of a DC current to heat the device using the losses [46] was used for the investigations in this section, with the electrical schematic and test setup shown in Figure 2.32 and Figure 2.33.

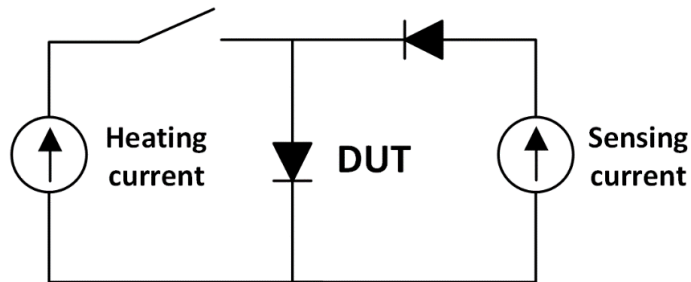


Figure 2.32 Electrical schematic of the DC power cycling test setup



Figure 2.33 Power cycling test setup

This method of power cycling involves injecting a heating current into the Device Under Test (DUT) to increase the junction temperature and using the forward voltage at a low Sensing Current as a TSEP. Since the sensing current is small and therefore cannot contribute to the temperature of the device, the on-state voltage measured in response to this sensing current is used as a TSEP, as defined previously in section 2.3.3.

The test set-up presented in Figure 2.32 and Figure 2.33 comprises of 2 power sources, one for producing the heating current and other for generating the sensing current. In order to use the forward voltage of the device as a TSEP, a calibration curve of the voltage as a function of temperature is first required as a reference. This involves measuring the forward voltage or on-state voltage at different temperatures when the device is in thermal equilibrium, to identify the relationship between the forward voltage and the temperature. The measured forward voltage or on-state voltage is compared with the initial calibration curve or look-up table and a temperature is inferred from the measured values. The calibration procedure can be done using a thermal chamber, a thermal bath or a hot plate (with different requirements for standardised measurements), but it is important to mention that the system used has to be in thermal equilibrium to allow the assumption of equal temperature between the device/module and the environment.

The switch shown in the test set-up is used to switch on and off the heating current and the auxiliary diode is used for decoupling both power supplies. When the transistor is switched on, the heating current is injected into the DUT for a time t_{on} and when the transistor is switched off the heating current is removed. The sensing current is always flowing through the DUT. The gate pulse of the transistor therefore determines the duty cycle of the DUT and can be used for adjusting the junction temperature (T_j) variation, as shown in Figure 2.34.

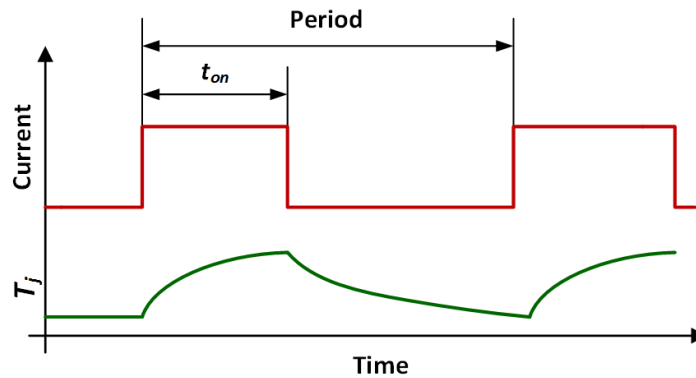


Figure 2.34 DC heating pulses and resulting junction temperature variation during power cycling

Once the heating current is removed, the junction temperature can be extracted using the calibrated TSEP [47]. This setup allows the characterisation of the thermal

resistance and the heating/cooling transients. In the case of the cooling transient, it is done capturing the voltage across the diode using the calibrated TSEP. For the heating transient, a sequence of short pulses is used for heating up the device, characterising the junction temperature after each pulse. The junction-to-case thermal resistance ($R_{th,j-C}$) of the device can be calculated by using a heating pulse with a known power P , which takes the device into thermal equilibrium. If the case temperature T_C is known, the thermal resistance can be estimated using equation (2.19). This characterisation can be performed at different intervals of the power cycling test to monitor the evolution of the thermal resistance as a function of the number of cycles.

$$R_{th,j-C} = \frac{T_j - T_C}{P} \quad (2.19)$$

The electrothermal performance during power cycling and its implications have been investigated for 600 V/4 A Silicon PiN from International Rectifier with datasheet reference HFA04TB60 and 600 V/4 A SiC Schottky diodes from CREE/Wolfspeed with datasheet reference C3D02060. These are discrete devices in a TO-220 package.

The calibration curve has been determined using a small hotplate to set the temperature of the device. This has been deemed suitable for this calibration given the reduced size of the discrete devices. Figure 2.35 shows the forward voltage measured at different temperatures for the SiC Schottky diode and the silicon PiN diode. It can be seen that the SiC device has a higher forward voltage compared to the silicon PiN diode and both diodes have a forward voltage with a negative temperature coefficient. The higher forward voltage in SiC is due to the wider bandgap, hence, the higher junction voltage. The SiC device also has a lower negative temperature coefficient compared to the silicon device. This is due to the lower intrinsic carrier concentration in SiC.

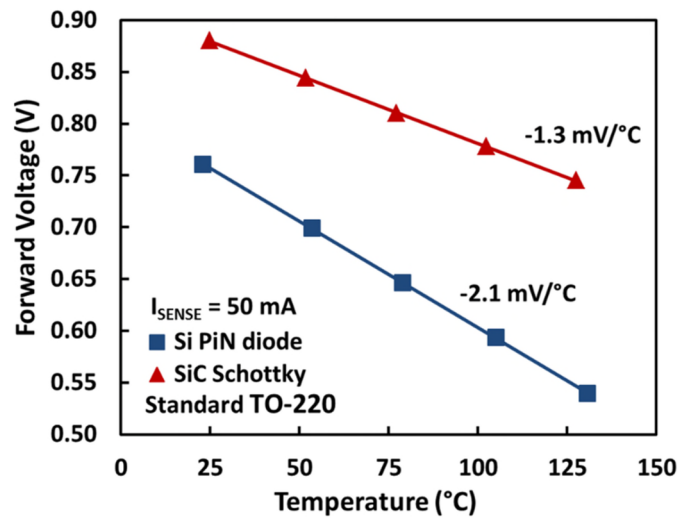


Figure 2.35 Calibration of the forward voltage as TSEP for the 600 V/4 A Si PiN and SiC Schottky diodes – (Standard TO-220 packages)

The availability of the same SiC Schottky diode die in two different packages allows the study of two packages with different thermal resistances. Both packaging alternatives are shown in Figure 2.36. The isolated version is completely encapsulated in the plastic insulator, hence, a higher thermal resistance is expected due to the lack of a good thermally conductive backside.

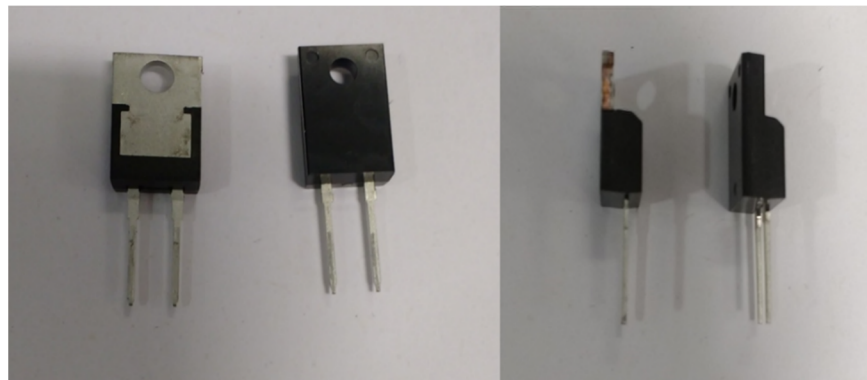


Figure 2.36 Standard and fully isolated TO-220 packages. Back and side views.

2.4.2 Electrothermal characterisation of Si PiN and SiC Schottky diodes

Using the setup presented in section 2.4.1, the thermal response of Si PiN and SiC Schottky diodes has been evaluated, characterising the response of the devices to defined DC heating pulses. For a single pulse, as defined in section 2.4.1, the junction temperature T_j will be controlled by the duration of the pulse t_{on} , the value of the heating current and

the electrothermal characteristics of the device under test. The internal PCB is shown in Figure 2.37.

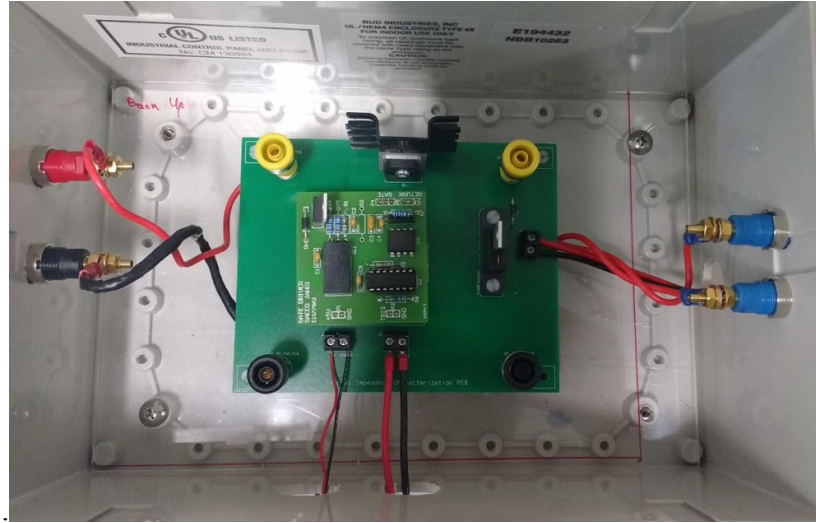


Figure 2.37 Detail of the power cycling PCB

Considering both Si and SiC devices direct replacements, from the application point of view, this strategy has been deemed suitable for the comparison of the electrothermal properties of both technologies, as the resulting junction temperature excursions will be determined by the characteristics of the device. Figure 2.38 shows the measured forward voltage using a 50 mA sensing current after 4 second heating pulses for three different DC heating currents, namely 1 A, 3 A and 5 A. Figure 2.38(a) shows the characteristics for the SiC Schottky diode while Figure 2.38(b) shows the characteristics for the silicon PiN diode. It can be seen that the forward voltage reduces with increasing heating current in both technologies, indicating a higher temperature as the sensing current is below the ZTC. The increase of the measured voltage is caused by the cooling of the device, with the minimum forward voltage corresponding to the maximum junction temperature. The forward voltages measured for the silicon PiN diode is also lower for the PiN diode compared with the SiC Schottky diode.

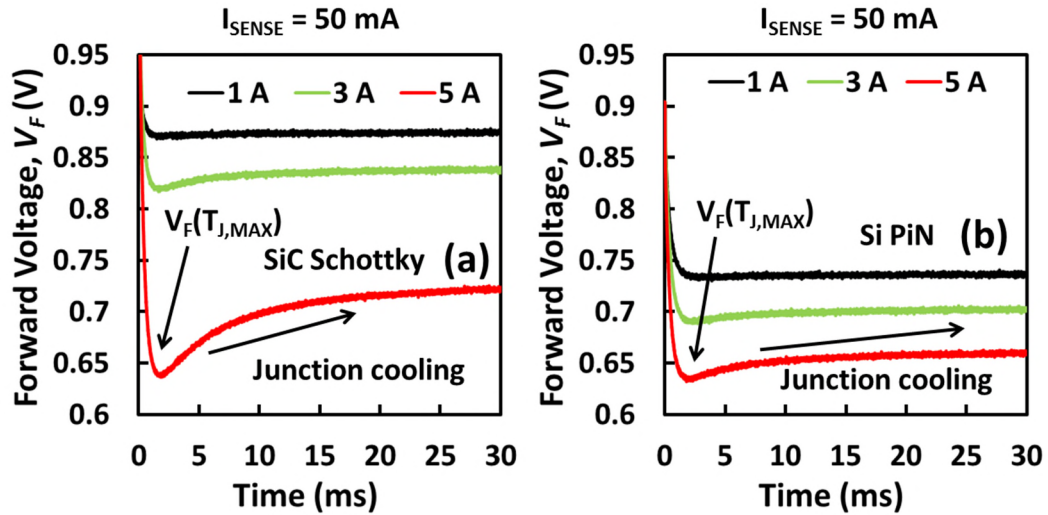


Figure 2.38 Forward voltage (TSEP) during the cooling of the Standard SiC Schottky (a) and Si PiN (b) after 4 second heating pulses

Using the calibrated TSEP, the junction temperature can be estimated from the measured transient voltage. This transient voltage was captured using an oscilloscope from Tektronix model TDS5054B and a differential probe from Pico Technology model TA043. A set of measurements was performed for different current levels (from 1 A to 5 A) and pulse durations (namely 1, 2 and 4 seconds). For these measurements, the devices were not attached to any heatsink and before each different pulse, the temperature of the device was taken to the ambient temperature, using the forward voltage as ambient temperature indicator.

The estimated junction temperature increase (ΔT_j) is summarised in Table 2-I for the SiC Schottky diode with datasheet reference C3D02060A and for the Si PiN diode with datasheet reference HFA04TB60.

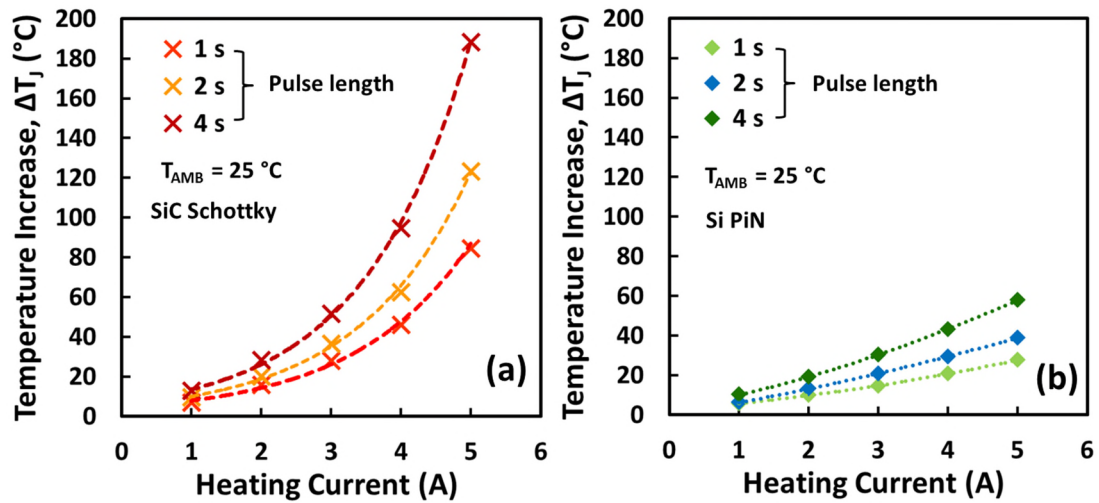
Table 2-I: Estimated junction temperature increase (ΔT_j) for the 600 V/ 4 A SiC Schottky diode for different heating pulses (duration and current level)

		Heating current (A)				
		1	2	3	4	5
Pulse width (s)	1	7.1	16.0	28.0	46.0	84.3
	2	9.6	20.0	36.6	62.6	123.3
	4	12.8	28.3	51.6	94.7	188.2

Table 2-II Estimated junction temperature increase (ΔT_j) for the 600 V/ 4 A Si PiN diode for different heating pulses (duration and current level)

		Heating current (A)				
		1	2	3	4	5
Pulse width (s)	1	5.8	10.0	14.5	20.9	27.6
	2	6.2	13.1	20.9	29.5	38.8
	4	10.2	19.1	30.4	43.2	57.9

Figure 2.39(a) shows the estimated junction temperature increase as a function of the heating current for different heating pulse durations in the case of the SiC Schottky, while Figure 2.39(b) shows similar measurements for the silicon PiN diode. It can be seen that the silicon device exhibits significantly less junction temperature increase compared to the SiC device for the same heating currents and heating durations.

**Figure 2.39 Junction temperature increase as a function of the heating current for the standard SiC Schottky (a) and Si PiN (b) diodes for heating pulse lengths**

This difference is due to the fact that SiC Schottky diodes have lower zero-temperature coefficients than silicon PiN diodes. Hence, for any of the heating currents evaluated, the forward voltage increases with temperature at a much higher rate in the SiC device compared to the silicon device. Since the silicon PiN diode has a high ZTC

point, the losses decrease with increasing temperature since the forward voltage decreases with increasing temperature.

Figure 2.40 presents data from Table 2-I and Table 2-II, but as a function of the heating time. It is clearly observed how at low heating current, namely 1 A and 2 A, the temperature increase can be considered similar for both technologies, SiC Schottky and Si PiN. However, as the heating current increases and its value is well above the zero temperature coefficient of the SiC Schottky, the impact of a longer heating pulse is clearly observed, as the results in Figure 2.40(a) show. Figure 2.40(b) shows the temperature increase for the Si PiN.

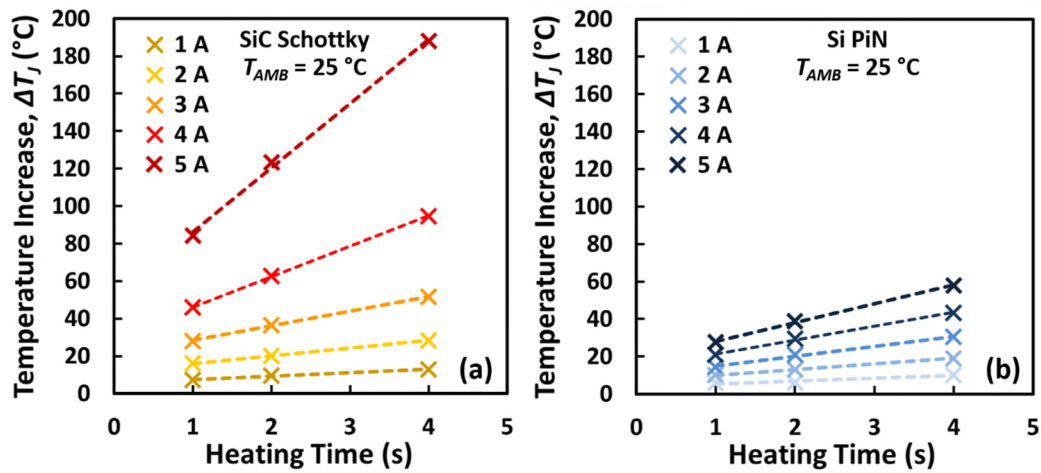


Figure 2.40 Junction temperature increase as a function of the heating time for the standard SiC Schottky (a) and Si PiN (b) diodes for different heating current levels

The measured forward voltage transients for the SiC and silicon devices are shown in Figure 2.41, for heating currents ranging from 1 A to 5 A and a heating pulse duration of 2 seconds. It is observed that the forward voltages are considerably higher for the SiC device compared to the silicon device, as well as the impact of the lower ZTC in the forward voltage for the SiC Schottky diode. From the results shown in Figure 2.41(a) it is clearly observed how for the silicon carbide Schottky diode increasing the current translates in a higher power pulse, which is considerably affected by the ZTC due to self-heating as the duration of the pulse increases.

In case of thermal impedance degradation during power cycling, this positive temperature coefficient will increase the power losses, leading to a higher temperature

which will have a positive feedback and will lead to an accelerated degradation, if the power dissipation or temperature excursion are not controlled [48].

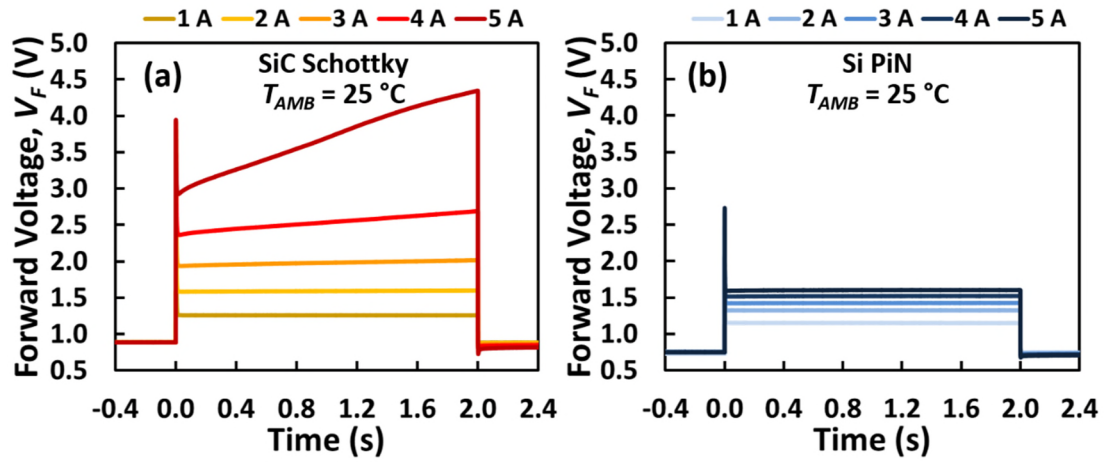


Figure 2.41 Forward voltage across the SiC Schottky diode (a) and the Si PiN diode (b) for 2 second heating pulses of different current levels

An interesting consideration would be the evaluation of the impact of the packaging degradation on the temperature increase for a determined heating pulse. This degradation can be emulated using the fully isolated SiC Schottky, where the heat transfer is impeded by the plastic encapsulation, leading to a higher thermal resistance. The device was subjected to the same evaluation pulses than the previous SiC Schottky diode and the results are presented in Table 2-III. The junction temperature increases for 1 s and 4 s heating pulses for both SiC Schottky diodes are compared in Figure 2.42, where it is clearly observed that the temperature increase is slightly higher for the fully isolated package.

Table 2-III Estimated junction temperature increase (ΔT_j) for the fully isolated 600 V/ 4 A SiC Schottky diode for different heating pulses (duration and current level)

		Heating current (A)				
		1	2	3	4	5
Pulse width (s)	1	10.1	19.8	32.6	53.0	93.1
	2	11.3	23.6	41.8	70.1	133.8
	4	13.9	31.6	57.2	104.2	198.7

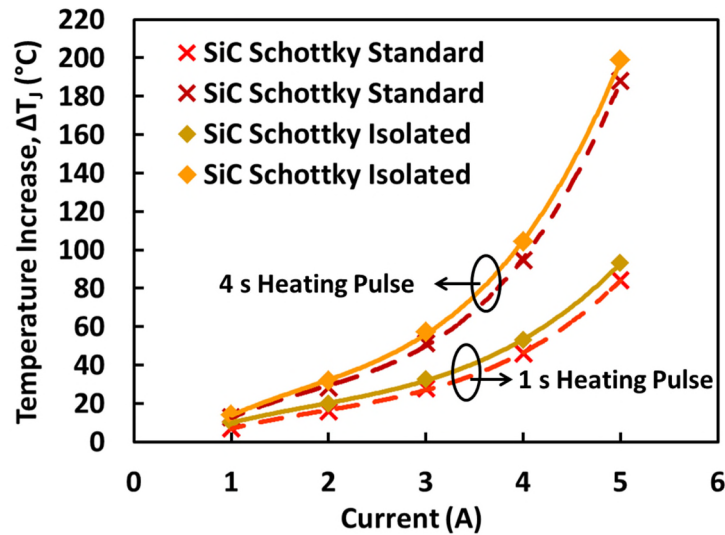


Figure 2.42 Junction temperature increase as a function of the heating current for the standard and fully isolated SiC Schottky diodes. Heating pulses of 1 s and 4 s.

The complete plastic encapsulation of the fully isolated SiC Schottky diode not only originates a higher thermal resistance. Compared with the standard TO-220, the isolated package will exhibit a different transient thermal impedance. This can be evaluated using the transient response to a heating pulse. Using the forward voltage as indicator of the junction temperature cooling, the forward voltage transient after a 4 seconds/ 5 A heating pulse is presented in Figure 2.43 for both SiC Schottky diodes. The peak value of V_F indicates the maximum junction temperature ($T_{j,max}$) and it is lower in the case of the fully isolated device.

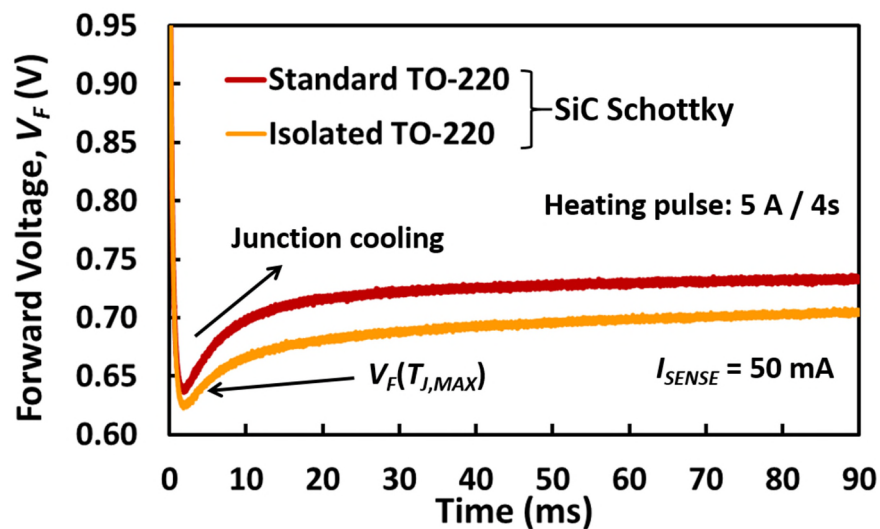


Figure 2.43 Forward voltage at low current (TSEP) during the cooling transient for the SiC Schottky diodes after a 4 s/5 A heating pulse

The different slopes of the forward voltage during the cooling transient indicate differences in the thermal flow between both devices, which could be characterised using the Cauer and Foster thermal models and the structure functions presented in chapter 1. The focus of this research is on the electrothermal properties of SiC and Si devices and the impact on power cycling, however, it is important to remark that information can be retrieved from the transient cooling.

2.4.3 Preliminary studies on power cycling

The availability of the same 600 V SiC Schottky diode in two different packaging alternatives (fully isolated TO-220 and standard TO-220) gives the opportunity of study the response of the packaging to power cycling tests. For this preliminary tests, the devices were attached to a small copper block of dimensions 20 mm x 11 mm x 3 mm used as heatsink. A high performance thermal pad model Sil-Pad 2000 for TO-220 devices from Bergquist was used for improving the heat transfer from the device to the copper block. For these preliminary tests natural convection was selected as cooling system and a picture of the assembly of the copper block and the device is shown in Figure 2.44.



Figure 2.44 Detail of the assembly of the discrete device for the power cycling tests

The power cycling strategy selected was constant heating/cooling times, as defined in chapter 1. The selected pulse was a 3 s heating pulse of 5 A followed by a 27 s cooling time, resulting in a power cycling period of 30 seconds. This pulse was generated using a Tektronix waveform generator model TDS2024C, which switched on and off the auxiliary device using a gate driver, as shown in Figure 2.37. For evaluating

the impact of the technology as well as the packaging, the use of a defined pulse with constant heating and cooling times, where the device characteristics together with the packaging properties would set the junction temperatures was deemed the most suitable strategy.

As it was mentioned before, the constant heating/cooling strategy will cause different junction temperature excursions for the different technologies evaluated. Using the voltage during the cooling transient, when the sensing current is flowing through the device, the junction temperature during this period can be estimated. The captured transient during the cooling period, when the device/heatsink assembly reached a steady state was recorded using a digital multimeter HAMEG model HMC 8012, with a sampling period of 5 milliseconds. The results are shown in Figure 2.45 for the 3 evaluated devices, and it is clearly observed how the Si PiN has a lower junction temperature excursion and average temperature. In the case of the SiC Schottky diodes, which are the devices of interest for this study, it is clearly observed that the isolated SiC Schottky diode has the highest junction temperature and junction temperature excursion. A different cooling transient is also observed by comparing both SiC devices, where the impact of the packaging limiting the heat extraction is clearly identified in the case of the isolated Schottky, indicating the impact of the packaging on the thermal properties of the discrete device.

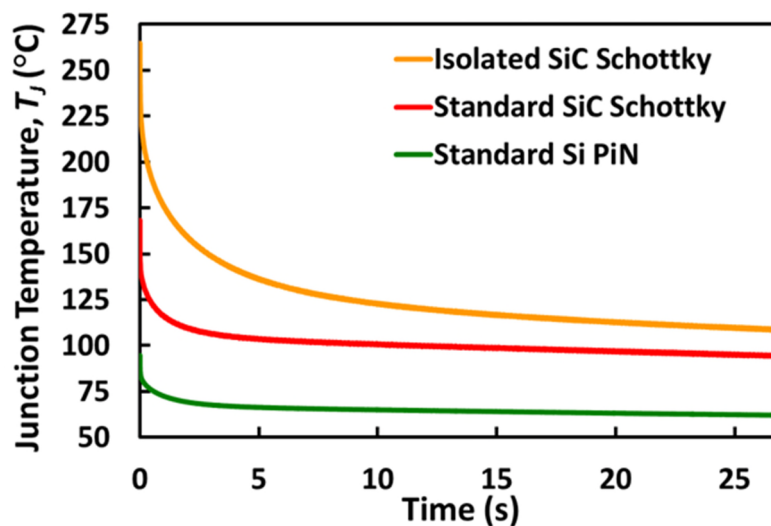


Figure 2.45 Junction temperatures excursions during the cooling period for the different evaluated technologies

Given the junction temperature excursions shown in Figure 2.45, subjecting the different devices to the same heating currents without controlling the case temperature or the junction temperature rise, would be a much harsher test for the SiC devices compared to the silicon devices. The resulting junction temperature excursions (ΔT_j) and medium temperatures (T_m), as defined in chapter 1, are summarised in Table 2-IV. These temperatures were estimated from the forward voltage, captured using a digital multimeter HAMEG HMC8012, with a sampling time of 5 ms. The transient waveforms presented in the previous section, were captured with an oscilloscope with a higher switching rate. The lower sampling rate of the multimeter can affect the measured peak junction temperature, however the trend and differences shown in Figure 2.45 are clear for the evaluated devices.

Table 2-IV: Junction temperature values (ΔT_j , $T_{j,max}$ and T_m) resulting from the power cycling tests of the different device technologies

	SiC Schottky Fully Isolated TO-220	SiC Schottky Standard TO-220	Si PiN Standard TO-220
Junction temperature excursion, ΔT_j (°C)	156.5	74.3	32.6
Maximum Junction Temperature, $T_{j,max}$ (°C)	264.4	168.0	94.7
Medium Junction Temperature, T_m (°C)	186.1	130.8	78.3

Power cycling tests were performed for both SiC Schottky diodes, with the thermal impedance characterised every 200 cycles, injecting a known power and taking the device to a steady state. Using equation (3.18) the thermal resistance can be calculated, with the junction temperature estimated using the calibrated TSEP, and the case temperature measured using a thermocouple attached to the copper block shown in Figure 2.46.

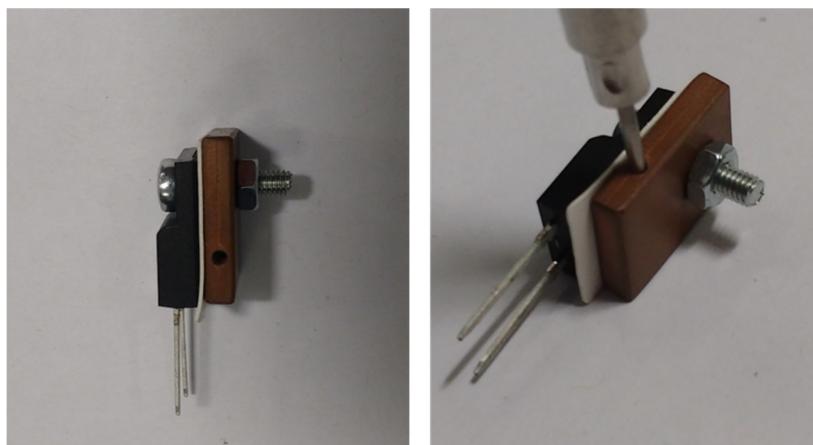


Figure 2.46 Detail of the hole in the copper block and thermocouple connection for measuring the case temperature

The results of these preliminary tests are shown in Figure 2.47, where the normalised thermal resistance is presented as a function of the number of cycles.

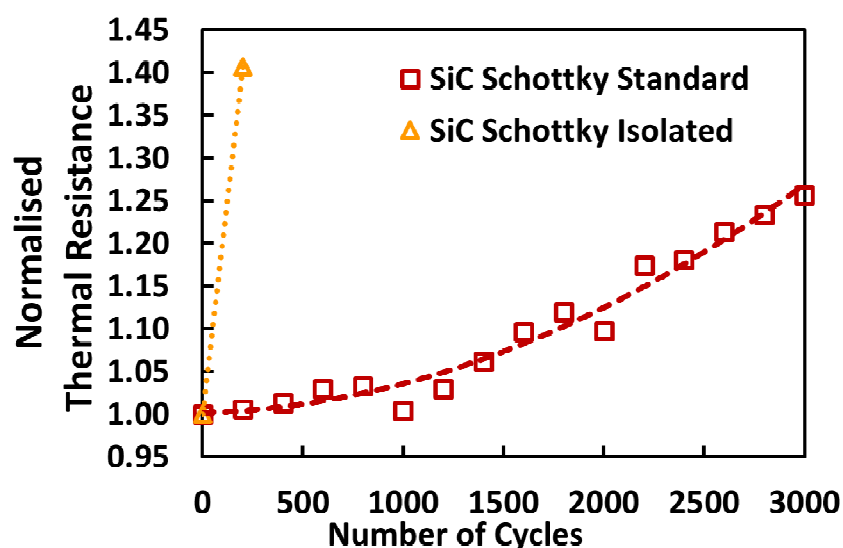


Figure 2.47 Thermal impedance during power cycling tests for the SiC Schottky diodes

As the results in Figure 2.47 show, the fully isolated device fails after 200 cycles, with an increase of thermal resistance of 40 %. In the case of the standard TO-220 packaged device, the nominal increase of the thermal resistance after 3000 cycles is 25.4%. As it was mentioned before, the considerable high temperature cycle imposed, translates into a short life time, clearly observed in the case of the fully isolated package.

The forward voltage and resistance of the devices subjected to power cycling were characterised at room temperature for a current of 2 A using a curve tracer Tektronix

model 371B. The results are shown in Table 2-V and show no noteworthy electrical degradation of the device.

Table 2-V Forward voltage and on-state resistance of the SiC Schottky diodes before and after the power cycling tests

	SiC Schottky Fully Isolated (0 cycles)	SiC Schottky Fully Isolated (200 cycles)	SiC Schottky Standard (0 cycles)	SiC Schottky Standard (3000 cycles)
Forward Voltage, $V_{F,I=2A}$ (V)	1.460	1.462	1.420	1.426
On-state resistance (Ω)	0.260	0.260	0.239	0.237

Power cycling is a time consuming, with 5 years of experiments reported in [49] and these initial tests would not be statistically representative, however some conclusions can be extracted from the presented results.

In the DC power cycling results presented in this chapter, the higher on-state voltage, together with the acceleration factor caused by a lower ZTC seem the factors which cause the SiC Schottky diodes to have a higher temperature cycle for the same heating current compared with the Si PiN diodes. This higher temperature cycle translates into higher thermomechanical stresses, which cause a lower power cycling capability of the devices.

From an application point of view, subjecting devices with different electrothermal characteristics to a defined mission profile [50] will cause different junction temperature excursions. Depending on factors like the conduction time, switching frequency and the converter topology evaluated the devices will dissipate different power losses, hence the junction temperature variations would be different. This has been evaluated for a 3 level NPC converter in [51], where the switching/conduction losses relationship seems a key factor for the selection of the devices of the converter. In this sense, it is important to acknowledge the impact that the change of device can have in other elements of the converter. If the complementary device is a PiN diode, the reverse recovery will affect the turn-on losses of the main switch [36]. Using the double pulse test setup presented previously in this chapter, the turn-on transient of a SiC MOSFET using a Si PiN diode and a SiC Schottky diode as clamping diode at different temperatures has been characterised. When a Si PiN diode is used, the increasing reverse recovery

current with temperature has an impact on the turn-on losses of the MOSFET as Figure 2.48(a) shows. However, in the case of the SiC Schottky the turn-on losses are not affected by the increasing temperature of the diode, as shown in Figure 2.48(b).

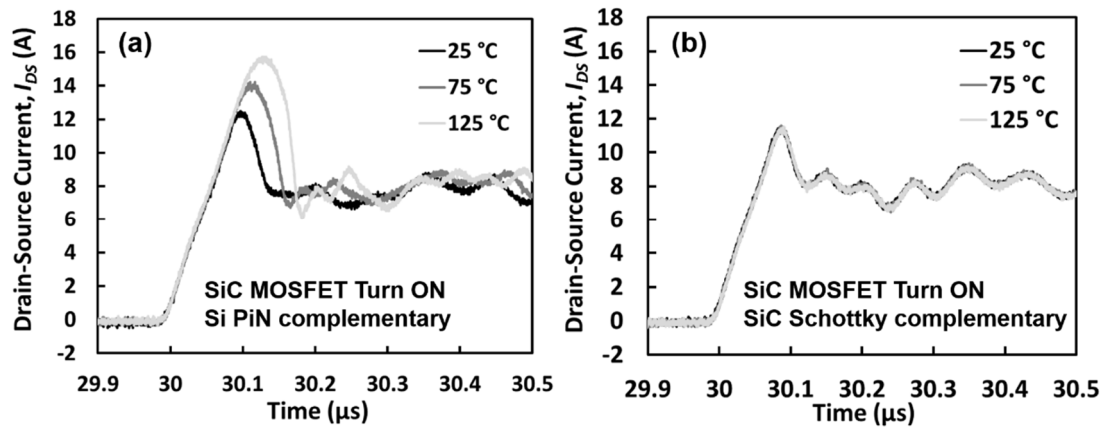


Figure 2.48 Turn-on current transient of a SiC MOSFET using (a) Si PiN diode as complementary device at different temperatures (b) SiC Schottky as complementary device at different temperatures

The lack of power cycling results for SiC devices compared with Si is a clear limitation for defining an empirical lifetime model, however in [52] the reduced power cycling capability of SiC diodes was identified and in [53] the authors evaluated the influence of the die material on the stresses on the solder. The different thermomechanical properties of SiC, including a 3 times higher Young's Modulus of compared to silicon and the smaller die size were cited as the possible reasons behind the reduced power cycling capability of packaging systems which were designed for silicon devices.

Using finite element analysis to model the different stresses on the packaging elements, from mapping the stresses on the solder, hence, the lifetime of silicon chips to silicon carbide chips [54] to the evaluation of the dimensions and material of the chip on the stresses on the solder [55].

Improvements on the packaging for SiC have been performed [56] and, as an example, a higher power cycling capability has been recently reported in [57]. The evolution of the SiC power modules is constant, however the new SiC power modules presented by different manufacturers [58, 59] are not widely commercially available.

2.5 Summary

In this chapter an overview of temperature sensitive electrical parameters for silicon power devices has been presented, focusing mainly on Si power devices. The electrothermal characterisation of SiC power devices is not as profuse as for Si power devices. Chapter 3 of this thesis will cover the electrothermal characterisation of SiC power devices, focusing on temperature sensitive electrical parameters of SiC power MOSFETs for condition monitoring.

Using the traditional DC power cycling test configuration, the different electrothermal characteristics of SiC Schottky diodes compared with Si PiN diodes, namely a higher on-state voltage and a lower zero temperature coefficient, cause the junction temperature increase to be higher when the devices are subjected to the same current pulse. This would lead to an accelerated degradation, especially if devices are considered a direct replacement.

A lower power cycling capability of power modules with SiC power devices has been identified as a major concern by different researchers, hence high reliability-high temperature packaging for SiC power devices is an active research area. Despite the new proposed packaging techniques, understanding the electrothermal performance of SiC power devices will be fundamental for implementing both effective online and offline condition monitoring strategies. Junction temperature is used for the identification of the thermal impedance degradation during power cycling tests (off-line) and it can enable condition monitoring based on junction temperature identification during online operation.

2.6 References

- [1] Flir. *Flir Infrared Cameras*. Available: <http://www.flir.co.uk/home/> (Access: 8/05/1017).
- [2] L. Dupont, Y. Avenas, and P. O. Jeannin, "Comparison of Junction Temperature Evaluations in a Power IGBT Module Using an IR Camera and Three Thermosensitive Electrical Parameters," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1599-1608, 2013.
- [3] A. Bryant, N. A. Parker-Allotey, D. Hamilton, I. Swan, P. A. Mawby, T. Ueta, *et al.*, "A Fast Loss and Temperature Simulation Method for Power Converters, Part I: Electrothermal Modeling and Validation," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 248-257, 2012.
- [4] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2901-2908.
- [5] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3099-3111, 2017.
- [6] K. Hamada, "Present Status and Future Prospects for Electronics in Electric Vehicles/Hybrid Electric Vehicles and Expectations for Wide-Bandgap Semiconductor Devices," in *Silicon Carbide*, ed: Wiley-VCH Verlag GmbH & Co. KGaA, 2009, pp. 1-19.
- [7] K. Wang, Y. Liao, G. Song, and X. Ma, "Over-Temperature protection for IGBT modules," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1-7.
- [8] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 17-27, 2014.
- [9] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 942-948.
- [10] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters; A review," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081-3092, 2012.
- [11] H. Niu and R. D. Lorenz, "Evaluating Different Implementations of Online Junction Temperature Sensing for Switching Power Semiconductors," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 391-401, 2017.

- [12] S. Jahdi, "Analysis of dynamic performance and robustness of silicon and SiC power electronics devices," PhD Thesis, School of Engineering, University of Warwick, 2016.
- [13] DBK. *PTC conductive heating elements*. Available: <https://www.dbk-group.com/uk/dbk-solutions/industrial-thermal-management/heating/ptc-conductive-heating-elements/conductive-heating-series/397/conductive-heating-series.html> (Access: 21/06/2017).
- [14] S. Bahl, "Application-Relevant Qualification of Emerging Semiconductor Power Devices," presented at the Applied Power Electronics Conference (APEC), 2016.
- [15] Cree/Wolfspeed. *SiC MOSFET Double Pulse Fixture*. Available: http://www.wolfspeed.com/downloads/dl/file/id/150/product/1/sic_mosfet_double_pulse_fixture.pdf (Access: 1/05/2017).
- [16] H. Luo, W. Li, and X. He, "Online high-power P-i-N diode chip temperature extraction and prediction method with maximum recovery current di/dt ," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2395-2404, 2015.
- [17] C. Zheng, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Master of Science in Electrical Engineering Department of Electrical Engineering, Virginia Polytechnic Institute and State University, 2009.
- [18] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 2681-2688.
- [19] Fred Wang, Zheyu Zhang, and Edward A. Jones, "Wide Bandgap Device Characterization," presented at the APEC, 2016.
- [20] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2008.
- [21] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors* 2nd ed.: SEMIKRON International GmbH, 2015.
- [22] N. Galanos, "Investigation of the inductor's parasitic capacitance in the high frequency switching of the high voltage cascode GaN HEMT," Master of Science Thesis, Department of Electrical Sustainable Energy, Delft University of Technology, 2015.
- [23] N. Baker, S. Munk-Nielsen, and S. Bęczkowski, "Test setup for long term reliability investigation of Silicon Carbide MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-9.
- [24] A. Koenig, T. Plum, P. Fidler, and R. W. D. Doncker, "On-line Junction Temperature Measurement of CoolMOS Devices," in *2007 7th International Conference on Power Electronics and Drive Systems*, 2007, pp. 90-95.
- [25] N. Baker, H. Luo, and F. Iannuzzo, "Simultaneous On-State Voltage and Bond-Wire Resistance Monitoring of Silicon Carbide MOSFETs," *Energies*, vol. 10, no. 3, p. 384, 2017.
- [26] R. Siemienieć, M. Netzel, and R. Herzer, "Comparison of PT and NPT cell concept for 600 V IGBTs," presented at the EPE Conference, Trondheim, 1997.
- [27] A. Sattar. *IXYS Application Note - Insulated Gate Bipolar Transistor (IGBT) Basics*. Available:

- http://www.ixys.com/Documents/AppNotes/IXYS_IGBT_Basic_I.pdf (Access: 20/06/2017).
- [28] E. R. Motto, J. F. Donlon, H. Takahashi, M. Tabata, and H. Iwamoto, "Characteristics of a 1200 V PT IGBT with trench gate and local life time control," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, 1998, pp. 811-816 vol.2.
 - [29] B. J. Baliga, "Chapter 2 - IGBT Structure and Operation," in *The IGBT Device*, ed Amsterdam: William Andrew Publishing, 2015, pp. 19-29.
 - [30] Fairchild Semiconductor, "AN-9106 - IGBT Basics Rev. 1.1," ed: Fairchild Semiconductor, 2016.
 - [31] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2011.
 - [32] W. Lai, M. Chen, L. Ran, S. Xu, N. Jiang, X. Wang, *et al.*, "Experimental Investigation on the Effects of Narrow Junction Temperature Cycles on Die-Attach Solder Layer in an IGBT Module," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1431-1441, 2017.
 - [33] M. A. Eleffendi, L. Yang, P. Agyakwa, and C. Mark Johnson, "Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement," *Microelectronics Reliability*, vol. 59, pp. 73-83, 4// 2016.
 - [34] S. Bęczkowski, P. Ghimre, A. R. d. Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online Vce measurement method for wear-out monitoring of high power IGBT modules," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-7.
 - [35] B. W. Williams, "Power Switching Devices and their Static Electrical Characteristics," in *Principles and Elements of Power Electronics*, B. W. Williams, Ed., 1 ed: Barry W Williams 2006.
 - [36] J. Hu, O. Alatisé, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Comparative electrothermal analysis between SiC Schottky and silicon PiN diodes: Paralleling and thermal considerations," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1-8.
 - [37] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power MOSFETs considering thermal aging effects," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 220-228, 2014.
 - [38] A. Bhalla. *Thermal resistance characterization of power MOSFETs*. Available: http://www.aosmd.com/res/application_notes/mosfets/character_mosfet.pdf (Access: 23/06/2017).
 - [39] L. Dupont, S. Lefebvre, M. Bouaroudj, Z. Khatir, J. C. Faugieres, and F. Emorine, "Ageing Test Results of low voltage MOSFET Modules for electrical vehicles," in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1-10.

- [40] M. A. Eleffendi and C. M. Johnson, "Evaluation of on-state voltage $V_{CE(ON)}$ and threshold voltage V_{TH} for real-time health monitoring of IGBT power modules," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 17th European Conference on*, 2015, pp. 1-10.
- [41] D. Barlini, M. Ciappa, M. Mermet-Guyennet, and W. Fichtner, "Measurement of the transient junction temperature in MOSFET devices under operating conditions," *Microelectronics Reliability*, vol. 47, no. 9–11, pp. 1707-1712, September 2007.
- [42] V. K. Sundaramoorthy, E. Bianda, R. Bloch, D. Angelosante, I. Nistor, G. J. Riedel, *et al.*, "A study on IGBT junction temperature (T_J) online estimation using gate-emitter voltage (V_{GE}) at turn-off," *Microelectronics Reliability*, vol. 54, no. 11, pp. 2423-2431, 2014.
- [43] A. Bryant, S. Yang, P. Mawby, D. Xiang, L. Ran, P. Tavner, *et al.*, "Investigation into IGBT dV/dt during turn-off and its temperature dependence," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3019-3031, 2011.
- [44] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5122-5132, 2016.
- [45] R. Bürkel and T. Schneider. *Fast Recovery Epitaxial Diodes (FRED) Characteristics - Applications - Examples. IXAN0044*. Available: <http://www.ixys.com/Documents/AppNotes/IXAN0044.pdf> (Access: 5/07/2017).
- [46] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power Cycle Testing of Power Switches: A Literature Survey," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2465-2473, 2015.
- [47] ABB, "Thermal design and temperature ratings of IGBT modules Application Note 5SYA 2093-00," ed: ABB, 2013.
- [48] U. Scheuermann and S. Schuler, "Power cycling results for different control strategies," *Microelectronics Reliability*, vol. 50, no. 9, pp. 1203-1209, 2010/09/01/ 2010.
- [49] U. Scheuermann. (2014, September) Reliability of Advanced Power Modules for Extended Maximum Junction Temperatures. *Bodo's Power*. 26-30.
- [50] M. Ciappa, "Lifetime prediction on the base of mission profiles," *Microelectronics Reliability*, vol. 45, no. 9, pp. 1293-1298, 2005/09/01/ 2005.
- [51] Z. Davletzhanova, O. Alatise, R. Bonyadi, S. Konaklieva, J. O. Gonzalez, L. Ran, *et al.*, "Electrothermal Stresses in SiC MOSFET and Si IGBT 3L-NPC Converters for Motor Drive Applications," presented at the Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), Nuremberg, 2017.
- [52] C. Herold, M. Schaefer, F. Sauerland, T. Poller, J. Lutz, and O. Schilling, "Power cycling capability of Modules with SiC-Diodes," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-6.
- [53] L. A. Navarro, X. Perpiñà, P. Godignon, J. Montserrat, V. Banu, M. Vellvehi, *et al.*, "Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap

- Semiconductor Devices and Harsh Environment Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2261-2271, 2014.
- [54] J. O. Gonzalez, L. Ran, A. M. M. A. Soli, Z. Davletzhanova, O. Alatise, P. Mawby, *et al.*, "Enabling high reliability power modules: A multidisciplinary task," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, 2016, pp. 1-5.
- [55] P. Rajaguru, H. Lu, C. Bailey, J. Ortiz-Gonzalez, and O. Alatise, "Evaluation of the impact of the physical dimensions and material of the semiconductor chip on the reliability of Sn3.5Ag solder interconnect in power electronic module: A finite element analysis perspective," *Microelectronics Reliability*, vol. 68, pp. 77-85, 1// 2017.
- [56] S. Seal and H. Mantooth, "High Performance Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions," *Energies*, vol. 10, no. 3, p. 341, 2017.
- [57] R. Schmidt, R. Werner, J. Casady, B. Hull, and A. Barkley, "Power Cycle Testing of Sintered SiC-MOSFETs," presented at the PCIM Europe, Nuremberg, Germany, 2017.
- [58] Y. Iwasaki, M. Chounabayashi, M. Nakazawa, S. Iwamoto, Y. Oonishi, M. Hori, *et al.*, "All-SiC Module with 1st Generation Trench Gate SiC MOSFETs and New Concept Package," presented at the PCIM Europe, Nuremberg, Germany, 2017.
- [59] T. Negishi, R. Tsuda, K. Ota, S. Iura, and H. Yamaguchi, "3.3-kV All-SiC Power Module for Traction System Use," presented at the PCIM Europe, Nuremberg, Germany, 2017.

3 Temperature Sensitive Electrical Parameters in Silicon Carbide Power Devices

3.1 Introduction

SiC power devices have demonstrated higher energy conversion efficiency and power density through reduced conduction and switching losses based on the material properties of silicon carbide [1]. SiC devices are gaining popularity and if their potential is to be maximised, the question of condition monitoring will become an important topic, as it has been discussed in chapter 1. Due to the wide bandgap in SiC (~ 3.3 eV), the intrinsic carrier concentration is lower and more thermal energy is needed to excite carriers across the bandgap. As a result, SiC devices allow operation at high temperature exceeding 200°C .

Different Temperature Sensitive Electrical Parameters (TSEPs) were presented in chapter 2, identifying the physics behind the temperature sensitivity of those parameters. Up to now, the temperature sensitivity of SiC devices has not been as widely studied as for Si devices and the available literature is sparser, however it is emerging as an important topic of research.

The forward voltage of a SiC Schottky diode exhibits good temperature sensitivity, for both low currents and high currents, as was evaluated in chapter 2, with a low zero temperature coefficient point, which will have a positive impact for paralleling of SiC Schottky diodes. This TSEP was characterised in chapter 2, where it was used for estimating the junction temperature during power cycling tests. In chapter 4 of this thesis, the forward voltage as TSEP for parallel diodes is studied in more depth.

The reverse recovery characteristics of a Si PiN diode during turn-off were presented as TSEP in the previous chapter, in section 2.3.6. The measured turn-off transient of a 600 V/15 A silicon PiN diode from International Rectifier, with datasheet number 15ETH06, is shown in Figure 3.1(a). The turn-off transient has been characterised at two different temperatures, namely 25°C and 100°C and it is clearly observed that the reverse recovery charge increases with temperature [2]. This is due to the positive temperature coefficient of minority carrier lifetime which has the effect to increase the stored charge in the diode drift region. Figure 3.1(b) shows the turn-off transient of a 600

V/9 A SiC Schottky diode from Cree/Wolfspeed with datasheet reference C3D06060A at 25 °C and 100 °C where it can be seen that there is no noticeable temperature sensitivity. This is absolutely beneficial from the point of view of switching losses, however it is a trade-off for estimating the junction temperature using TSEPs.

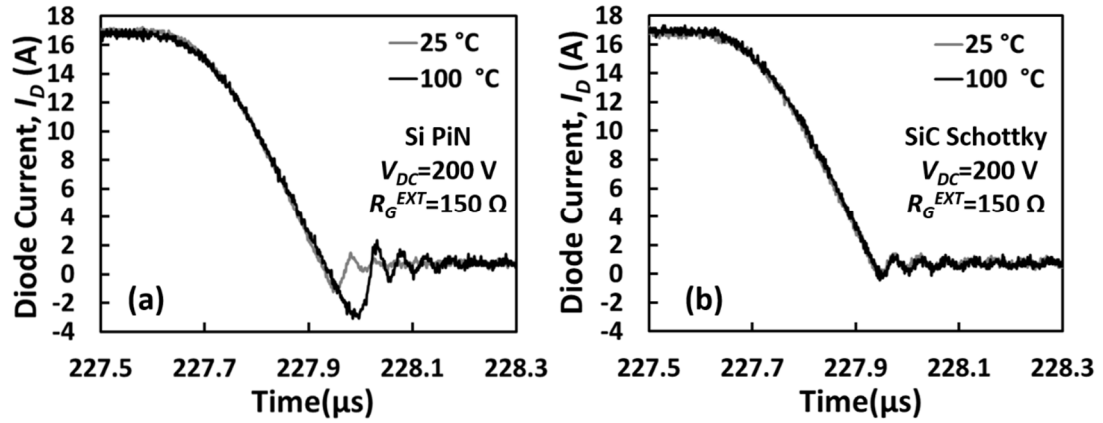


Figure 3.1 (a) Turn-off current transient of a Si PiN diode, (b) Turn-off current transient of a SiC Schottky diode

The complementary device used for these switching measurements is a 1200 V/42 A SiC MOSFET from Cree/Wolfspeed with datasheet number CMF20120D, driven with a gate driver voltage $V_{GG}=17$ V and a gate resistance R_G^{EXT} of 150 Ω . Increasing the switching rate by means of reducing the gate resistance will have an impact on the reverse recovery of the diode, as described in [3]. This is shown in Figure 3.2(a) for a PiN diode, where the turn-off transient of the diode current is shown for 3 different switching rates. It is clearly observed that the reverse recovery characteristics are influenced by the complementary switching device. In the case of the evaluated SiC Schottky diode, despite the increase of the switching rate during the turn-off transient, there is no noteworthy impact on the switching characteristics, as the results in Figure 3.2(b) show.

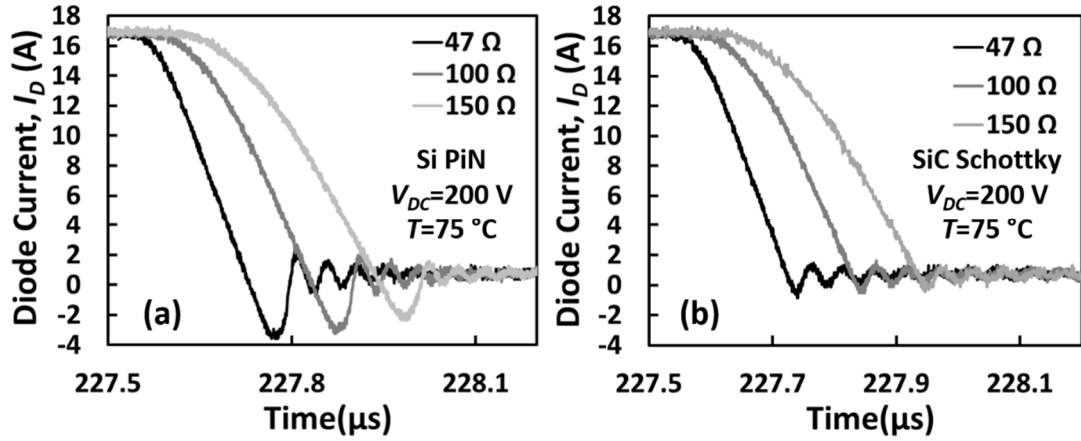


Figure 3.2 Impact of the switching rate of the complementary transistor on the turn-off current transient: (a) Si PiN diode (b) SiC Schottky diode

The results for both diodes are presented together in Figure 3.3, where it can be easily identified which part of the transient is determined by the recovery characteristics of the diode and which part is determined by the switching rate of the complementary transistor, as presented in chapter 2.

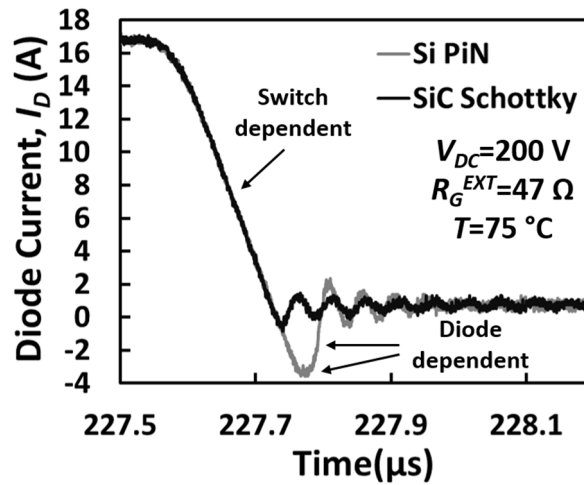


Figure 3.3 Impact of the complementary switch properties and the diode properties on the turn-off transient of a Si PiN diode and a SiC Schottky diode

Referring back to chapter 2, where the on state resistance as TSEP was analysed for silicon MOSFETs, in the case of SiC MOSFETs the temperature dependency of the on-state resistance is not linear and is low [4].

Measurements of the on-state resistances for different MOSFET technologies at different temperatures are shown in Figure 3.4, where the values of R_{DS-ON} have been normalised respect to the value measured at the ambient temperature T_{AMB} of 25 °C. The results presented in Figure 3.4 have been obtained using a gate-source voltage (V_{GS}) of

17 V and they have been measured at low current to avoid the self-heating of the devices. The test setup was presented in chapter 2, where the system for adjusting the temperature of the device was also defined. The evaluated devices include two 1200 V SiC MOSFETs (from Cree/Wolfspeed with datasheet reference CMF10120D and C2M0160120D), a 1200 V silicon MOSFET (from IXYS with datasheet reference IXFX20N120P) and a 900 V COOLMOS device (from Infineon with datasheet reference IPW90R340C3). It can be seen that the SiC MOSFETs show the lowest temperature sensitivity as far as the on-state resistance is concerned, with the Cree/Wolfspeed second generation device showing higher temperature sensitivity than the first generation due to the improved channel resistance [4].

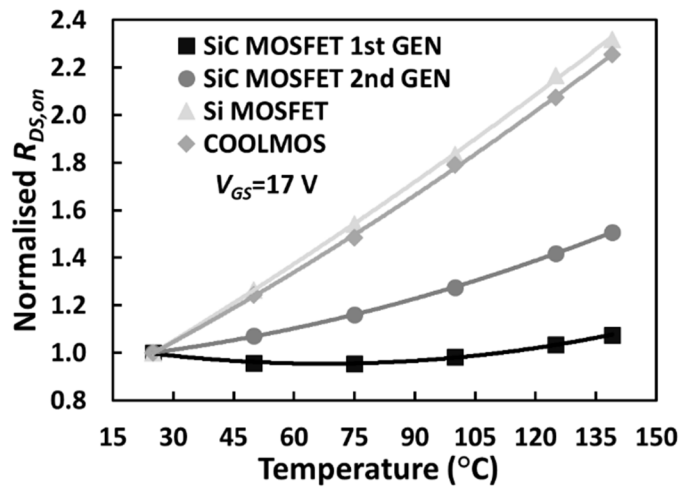


Figure 3.4 Normalised on-state resistance as a function of temperature for different MOSFET technologies

Compared with IGBTs, where the on-state voltage at low currents would be a good TSEP, in the case of MOSFETs its application as TSEP could be difficult given the lower value of the measured voltage. At high currents, the temperature sensitivity is clearly observed for Si MOSFETs and it has been already used in [5] for a COOLMOS device. The forward voltage at high currents, measured during self-heating is presented in Figure 3.5, for the two different generation SiC MOSFETs and the Si COOLMOS.

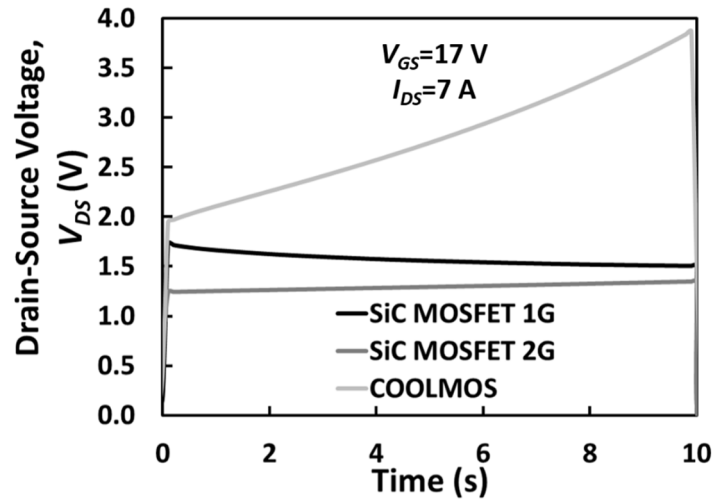


Figure 3.5 On-state voltage (V_{DS}) at high current during a heating pulse for different MOSFET technologies

In the case of the 1st Generation SiC MOSFET, the impact of the negative and positive temperature coefficients of the on-state resistance is easily identified in Figure 3.6. For these measurements a longer duration of the heating pulse was used, hence causing a higher junction temperature increase. As the normalised results presented in Figure 3.4 already indicated, the temperature sensitivity is low and the same forward voltage can be measured for two different temperatures.

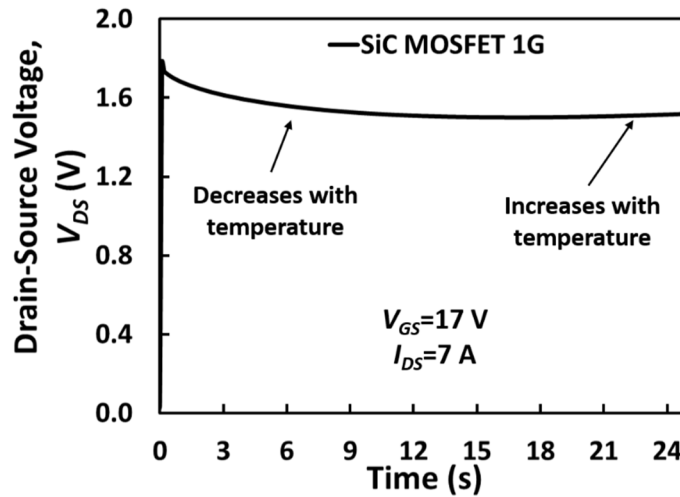


Figure 3.6 On-state voltage (V_{DS}) at high current during a heating pulse for a SiC MOSFET

The normalised on-state resistance results presented in Figure 3.4 were obtained for a gate-source voltage V_{GS} of 17 V and the change of the temperature coefficient with temperature, from negative to positive, is clearly observed. An interesting observation is that in the case of SiC MOSFETs, compared with Si MOSFETs, a higher gate to source voltage is required to obtain a low value for the on-state resistance [4]. The impact of the

gate drive voltage on the on-state resistance of SiC MOSFETs and its temperature sensitivity would be evaluated in chapter 4.

At low sensing currents, the parasitic body diode of a MOSFET can be used as a temperature indicator, given the temperature sensitivity of the p-n junction. The physics behind this temperature sensitivity were described in the chapter 2, in section 2.3.3. The forward voltage across the body diode of a SiC MOSFET from Cree/Wolfspeed with datasheet number C2M0280120D has been calibrated as TSEP, using experimental setup and calibration procedure defined in chapter 2, for a sensing current I_{SENSE} of 50 mA. The gate and source terminal were shorted, hence the resulting gate-source voltage V_{GS} was 0 V. A negative temperature coefficient is clearly observed for this TSEP.

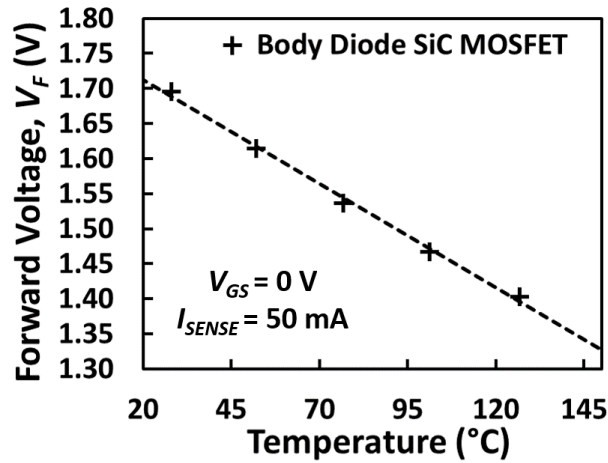


Figure 3.7 Calibration curve of the voltage across the body diode of a SiC MOSFET at different temperatures, for a current of 50 mA

The turn-off delay is a good TSEP for silicon IGBTs and MOSFETs as it was analysed in the previous chapter, in section 2.3.5. The impact of the temperature on the turn-off delay can be observed in the gate voltage and the device current. In the case of silicon IGBTs, the duration of the Miller plateau has a good temperature sensitivity, which can be improved if the device is slowed down by means of increasing the gate resistance.

Figure 3.8, Figure 3.9 and Figure 3.10 present the gate voltage and drain-source voltage during the turn-off transient of a SiC MOSFET, a silicon IGBT and a silicon MOSFET respectively. The devices selected are 1200 V rated with similar current ratings. The datasheet references of the selected devices are CMF10120D for the SiC MOSFET, IGW15T120 for the IGBT and IXFX20N120P for the Si MOSFET.

Evaluating the turn-off transient of a SiC MOSFETs, the lack of a clearly defined flat Miller plateau is clearly observed, together with a noteworthy reduction of the “plateau” duration, compared with the silicon IGBT and silicon MOSFET. As it is clearly observed in the gate voltage plots below, the turn-on voltage is 17 V and the turn-off voltage is 0 V.

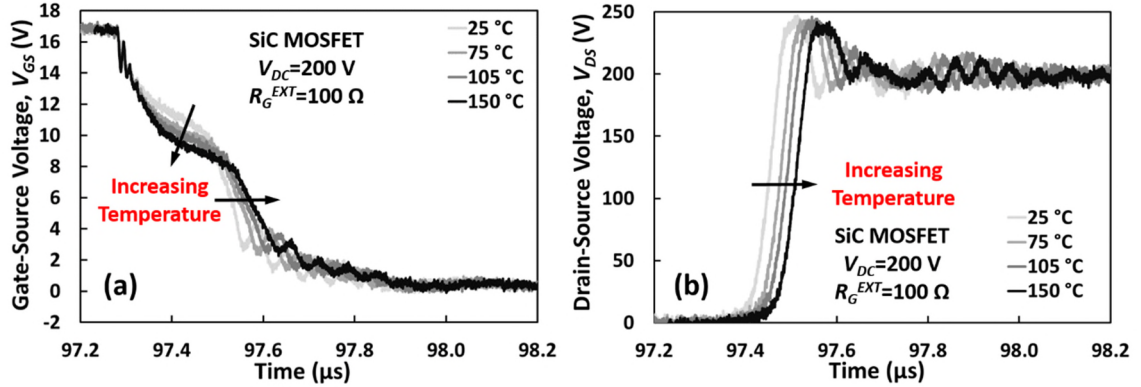


Figure 3.8 Turn-off transient of a SiC MOSFET at different temperatures: (a) Gate voltage, (b) Drain-Source Voltage

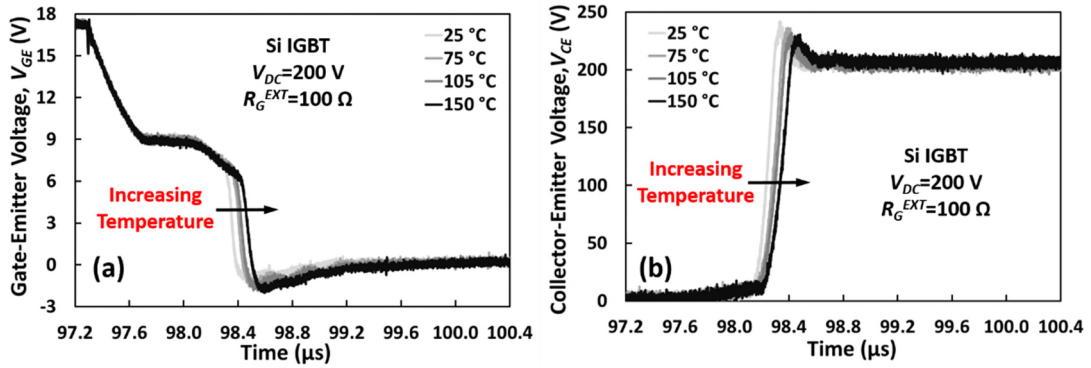


Figure 3.9 Turn-off transient of a Si IGBT at different temperatures: (a) Gate voltage, (b) Collector-Emitter Voltage

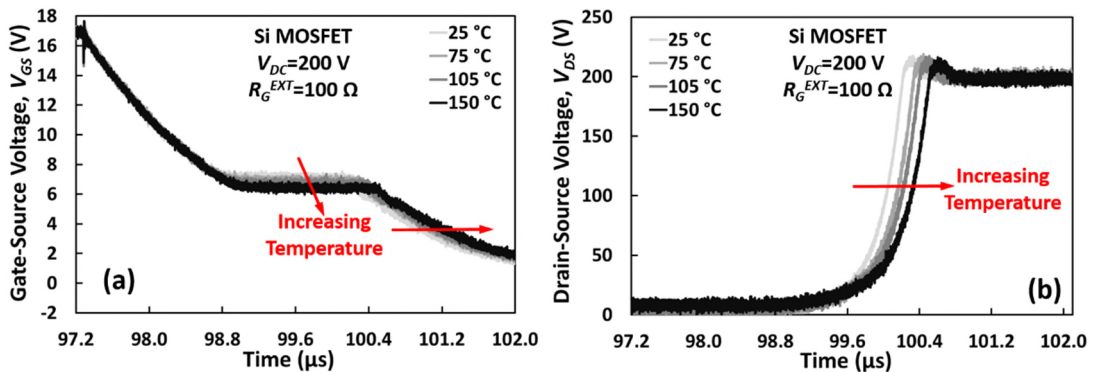


Figure 3.10 Turn-off transient of a Si MOSFET at different temperatures: (a) Gate voltage, (b) Drain-Source Voltage

The impact of the parasitic capacitances, determined by the size of the chip, is clearly observed in the turn-off transient of the gate voltage. The three devices are switched off with an external gate resistance R_G^{EXT} of 100 Ω , hence the different duration of the switching time constant is defined by the parasitic capacitances and internal gate resistances. This is particularly noticeable for the Si MOSFET, which according to the datasheet has an input capacitance C_{ISS} of 11.1 nF.

The duration of the plateau is clearly affected by the junction temperature for silicon IGBTs, together with the reduction of the turn-off switching rate of the collector-emitter voltage, as the measurements in Figure 3.9 show. In the case of the silicon and silicon carbide MOSFETs, the switching rate of the drain-source voltage is not noticeably affected, but it is clearly observed how it is shifted in time, indicating a longer turn-off transient.

Analysing the turn-off transient globally, the junction temperature can be evaluated using the delay time before the current goes to zero, starting from the instant when the gate is switched-off. This delay time has been used as TSEP in [6], where the voltage across the stray inductance is utilised as sensor.

Figure 3.11 presents the measured turn-off transient of the current for a silicon IGBT and Silicon MOSFET. In the case of the IGBT, the characteristic “tail current” is clearly identified Figure 3.11(a).

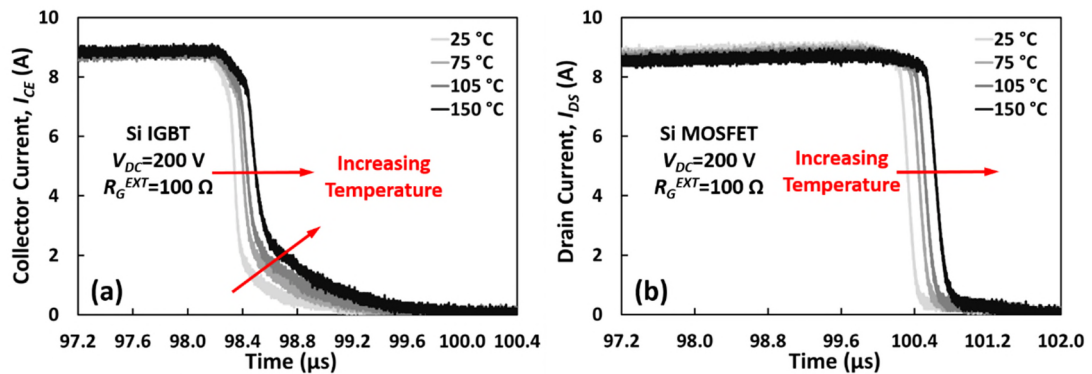


Figure 3.11 Turn-off current transient at different temperatures. (a) Si IGBT (b) Si MOSFET

The measured turn-off transient of the drain current of a SiC MOSFET is shown in Figure 3.12. Figure 3.12 (a) shows the results for an external gate resistance of 100 Ω , while Figure 3.12 (b) presents the measured transient for an external gate resistance of 220 Ω . It is clearly observed how the impact of the reduced parasitic capacitances

compared with a silicon MOSFET and a silicon IGBT result in a faster turn-off transient. The temperature sensitivity is also improved if the device is switched off with a larger external gate resistance.

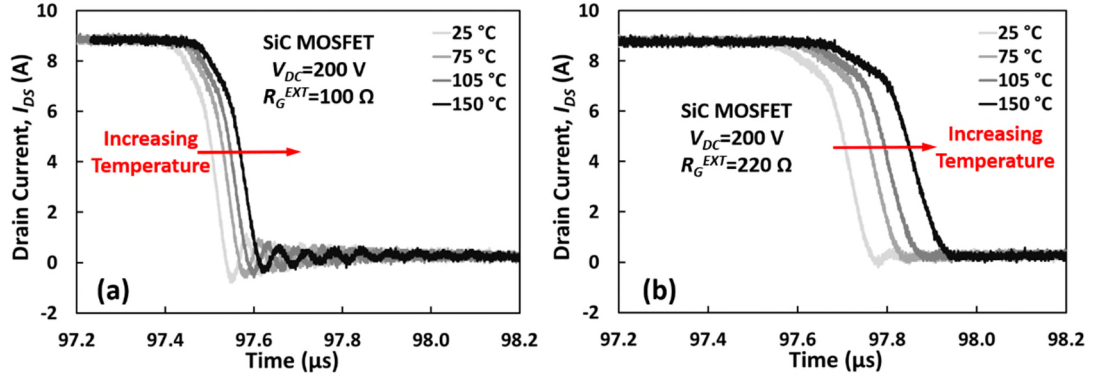


Figure 3.12 Turn-off current transient of a SiC MOSFET at different temperatures. (a) Gate resistance $R_G^{EXT}=100\ \Omega$, (b) Gate resistance $R_G^{EXT}=220\ \Omega$

An interesting observation identified by different researchers [7, 8], is that the switching rate of the drain current of silicon carbide MOSFETs during the turn-on transient increases with temperature. The turn-on transient of the previously evaluated devices, is shown in Figure 3.13 for the silicon IGBT and silicon MOSFET switched with a gate resistance R_G^{EXT} of $47\ \Omega$. From the captured transients, it is clearly observed how in the case of the IGBT and the MOSFET the turn-on transient shifts in time, caused by a lower threshold voltage, as it was explained in the previous chapter, in section 2.3.4. In the case of the IGBT, the collector current switching transient shows both positive and negative temperature coefficients [9], while in the case of the silicon MOSFET the switching rate is apparently constant or reduces slightly.

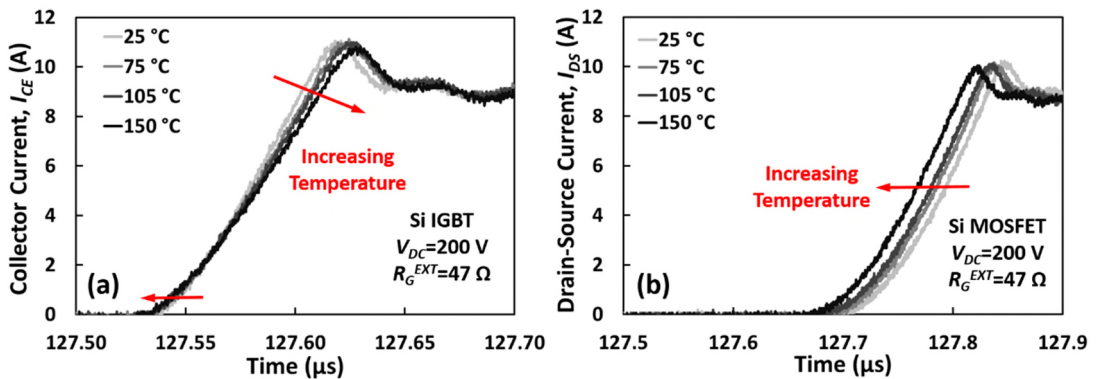


Figure 3.13 Turn-on current transient of (a) Si IGBT, $R_G^{EXT}=47\ \Omega$, (b) Si MOSFET, $R_G^{EXT}=47\ \Omega$

The turn-on transient of the 1200V/24A SiC MOSFET with datasheet reference CMF10120D is shown in Figure 3.14, where the increasing switching rate with temperature is clearly observed, together with the shift in time of the turn-on transient caused by the lower threshold voltage with temperature.

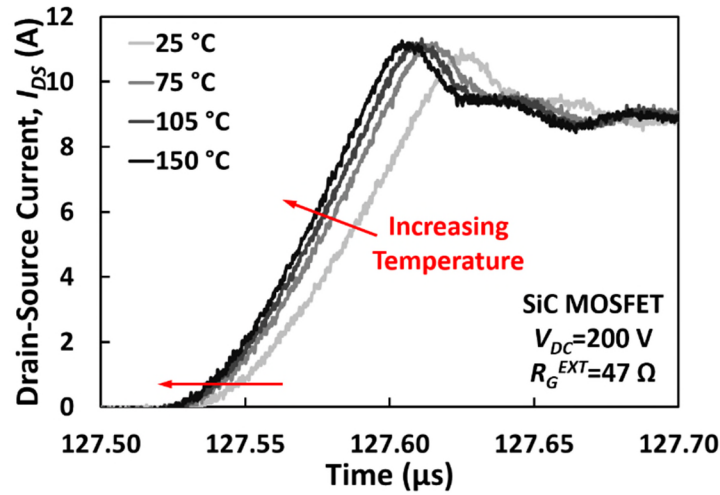


Figure 3.14 Turn-on current transient of a SiC MOSFET, $R_G^{EXT}=47\ \Omega$,

The impact of the junction temperature on the switching transient is clearly observed in Figure 3.15(b), when SiC MOSFET is switched with an external gate resistance R_G^{EXT} of 220 Ω . The impact of the lower threshold voltage shifting the transient to the left and the increase in the switching rate are more pronounced when the device is driven slowly. However, the temperature sensitivity of the switching rate is noticeably reduced when the device is switched using a 10 Ω gate resistance, as the captured transient in Figure 3.15(a) shows. The turn-on transients were measured with a Tektronix current probe model TCP-312, with a bandwidth of 100 MHz and a rise time of 3.5 ns.

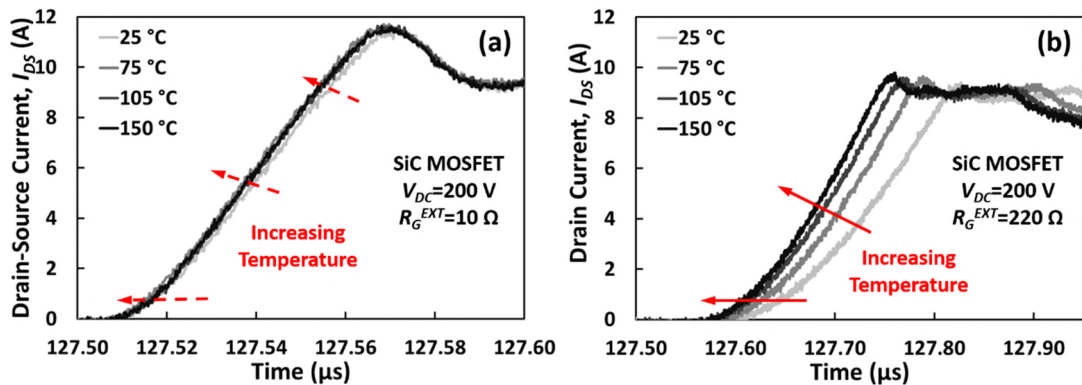


Figure 3.15 Turn-on current transient of a SiC MOSFET, (a) $R_G^{EXT}=10\ \Omega$, (b) $R_G^{EXT}=220\ \Omega$

The impact of the increased switching rate is also noticeable in the turn-on transient of the drain-source voltage, as the results in Figure 3.16 show.

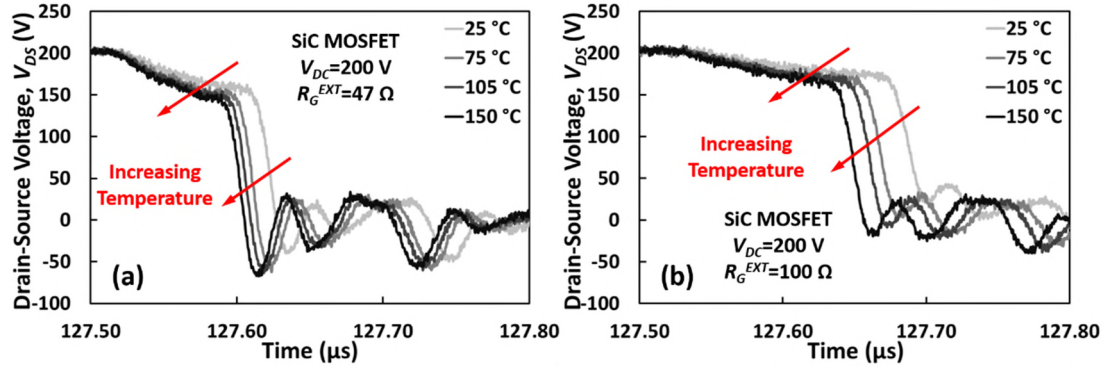


Figure 3.16 Turn-on voltage transient of a SiC MOSFET, (a) $R_G^{EXT}=47\ \Omega$, (b) $R_G^{EXT}=100\ \Omega$

The initial dip in the drain-source voltage is caused by the current rising [10] and the inductance in the measurement path, which includes the parasitic inductance of the packaging and the stray inductance between the measurement points and the packaged device. Measuring the voltage across the stray inductance of the package if an auxiliary connection is available is a technique which has been used in advanced gate drivers in for achieving closed loop dI/dt control [11] and characterising the impact of temperature in different TSEPs [3, 6].

3.2 Analytical modelling of gate and drain current transients in SiC power MOSFETs

As it has been presented in the section 3.1, it is a general observation that the current commutation rate (dI_{DS}/dt) increases with temperature during the turn-on transient of SiC power MOSFETs [7, 8], however, what has not been adequately investigated is the impact of temperature on the gate current plateau and how this, together with the turn-on dI_{DS}/dt can be used as a TSEP for junction temperature identification in SiC power MOSFETs.

The turn-on of a MOSFET is described in [10, 12, 13]. The idealised plots of the gate current (I_G), the drain-source current (I_{DS}) and the gate-source voltage (V_{GS}) transients for a SiC MOSFET during turn-on at a low (25°C) and high (150 °C) junction temperatures are shown in Figure 3.17(a). Figure 3.17 (b) shows experimental measurements for a 1200 V/42 A SiC MOSFET from Cree/Wolfspeed with datasheet

reference CMF20120D. The transient was measured using the double pulse configuration described in chapter 2.

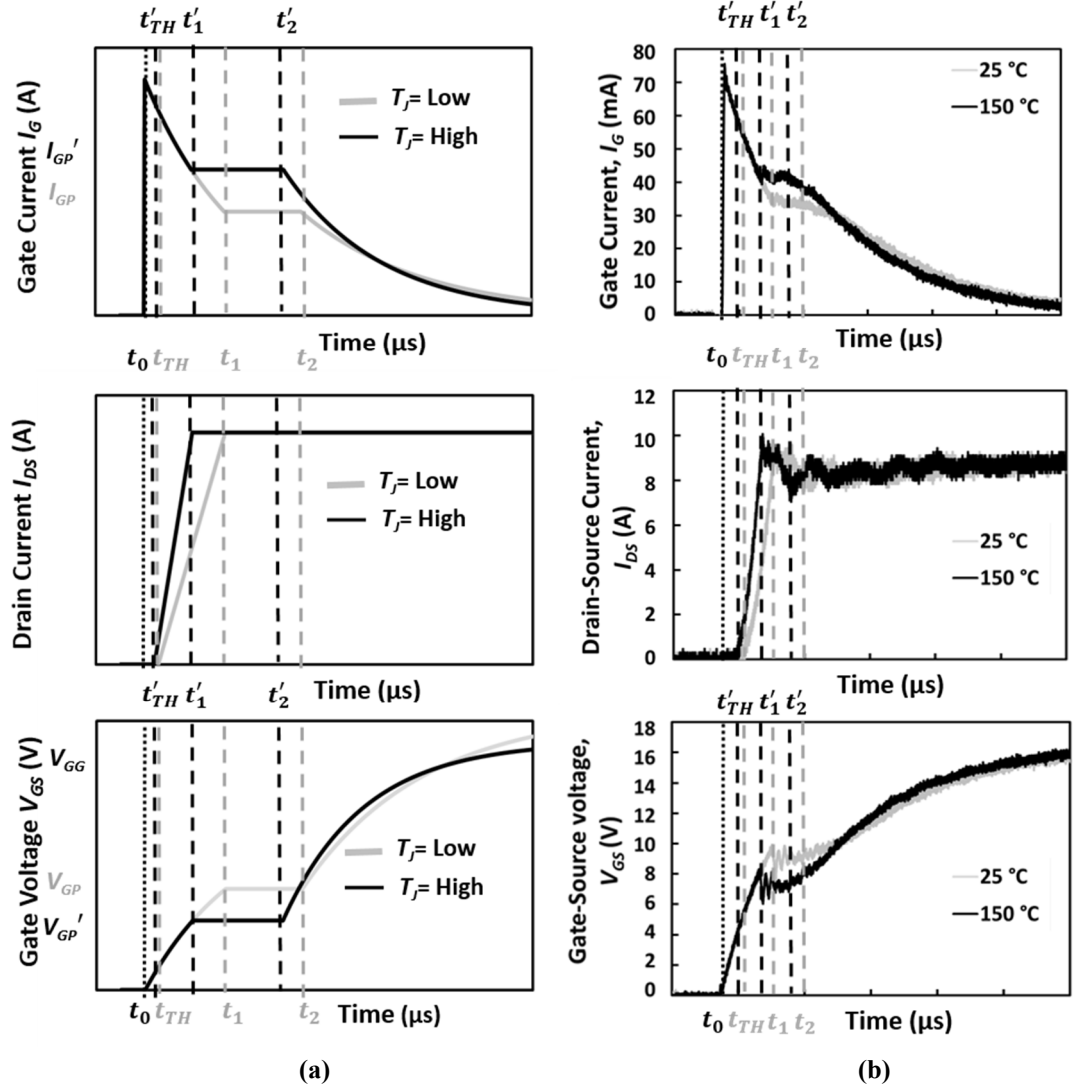


Figure 3.17 (a) Idealised I_G , I_{DS} and V_{GS} turn-on transients for a SiC MOSFET at different temperatures, (b) Measured I_G , I_{DS} and V_{GS} turn-on transients for a SiC MOSFET at different temperatures

As the measurements show, the turn-on dI_{DS}/dt and the gate-current plateau (I_{GP}) both increase with temperature, whereas the gate voltage plateau (V_{GP}) reduces with increasing temperature. During the turn-on transient of the SiC MOSFET, the total gate current supplied by the gate driver is given by the time dependent combination of 3 stages described by equation (3.1), where I_G is the total gate current, C_{GS} is the gate source capacitance, C_{GD-HV} is the Miller capacitance at high drain voltage, C_{GD-LV} is the Miller capacitance at low drain voltage, V_{GG} is the gate drive voltage, R_G^{EXT} is the external gate resistance, R_G^{INT} is the internal gate resistance and V_{GP} is the plateau voltage.

$$I_G = \begin{cases} \frac{C_{GS}}{(C_{GS} + C_{GD-HV})} \frac{V_{GG}}{(R_G^{INT} + R_G^{EXT})} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT})(C_{GS} + C_{GD-HV})}} & \text{for } t_0 < t < t_1 \\ \frac{V_{GG} - V_{GP}}{R_G^{INT} + R_G^{EXT}} & \text{for } t_1 < t < t_2 \\ \frac{C_{GS}}{(C_{GS} + C_{GD-LV})} \frac{V_{GG} - V_{GP}}{(R_G^{INT} + R_G^{EXT})} e^{-\frac{t-t_2}{(R_G^{INT} + R_G^{EXT})(C_{GS} + C_{GD-LV})}} & \text{for } t_2 < t < t_3 \end{cases} \quad (3.1)$$

Assuming that the MOSFET gate is triggered at time t_0 according to Figure 3.17, between time t_0 and t_1 , the gate current charges the input capacitance C_{ISS} which is given by the sum of the gate-source capacitance (C_{GS}) and the Miller capacitance (C_{GD}).

$$C_{ISS} = C_{GS} + C_{GD} \quad (3.2)$$

Depending on the RC time constant of the gate transient, V_{GS} will reach V_{TH} at time t_{TH} which is between t_0 (when the gate is triggered) and t_1 (when $V_{GS} = V_{GP}$). The load current starts to rise at time t_{TH} and reaches its maximum at t_1 , causing the V_{DS} across the MOSFET to fall to its on-state value thereby charging the Miller capacitance between t_1 and t_2 . The threshold voltage and time it takes for V_{GS} to rise to V_{TH} ($t_{TH} - t_0$) have already been presented as TSEPs for silicon MOSFETs in chapter 2, section 2.3.4. Equation (3.3) models t_{TH} .

$$\begin{aligned} t_{TH} - t_0 &= (R_G^{INT} + R_G^{EXT}) C_{ISS} \ln \left(\frac{V_{GG}}{V_{GG} - V_{TH}} \right) = \\ &= (R_G^{INT} + R_G^{EXT}) C_{ISS} \ln \left(\frac{V_{GG}}{V_{GG} - \left(V_{TH}|_{25^\circ C} - \left| \frac{dV_{TH}}{dT} \right| (T_j - 25) \right)} \right) \end{aligned} \quad (3.3)$$

As I_{DS} reaches the load current I_{LOAD} , V_{GS} reaches its plateau value (V_{GP}) and the gate current reaches its plateau value (I_{GP}). The gate voltage plateau (V_{GP}) is given by equation (3.4)

$$V_{GP} = V_{TH} + \sqrt{\frac{I_{LOAD} L_{CH}}{\mu_{ni} C_{OX} W_{CH}}} \quad (3.4)$$

where μ is the effective mobility, W_{CH} the MOSFET channel width, C_{OX} the gate oxide capacitance density and L_{CH} the MOSFET channel length. The 2 temperature sensitive parameters that determine the value of V_{GP} in equation (3.4) are the threshold voltage (V_{TH}) and the effective mobility of the electrons in the channel of the MOSFET (μ). V_{TH} reduces with temperature as a result of temperature induced bandgap narrowing, which increases the intrinsic carrier concentration of the semiconductor thereby making the channel easier to invert [12]. The temperature dependency of V_{TH} is given by equation (3.5).

$$\frac{dV_{TH}}{dT} = \frac{d\psi_B}{dT} \left(2 + \frac{1}{c_{OX}} \sqrt{\frac{\epsilon_{SiC} q N_A}{\psi_B}} \right) \quad (3.5)$$

where

$$\frac{d\psi_B}{dT} \approx \frac{1}{T} \left[\frac{E_g(0)}{2q} - |\psi_B| \right] \quad (3.6)$$

ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level, ϵ_{SiC} is the dielectric constant of silicon carbide, N_A the doping density, q the electron charge and $E_g(0)$ the band-gap energy at $T=0$ K. According to the datasheets and previously presented measurements [14, 15] the threshold voltage is higher for Si MOSFETs however, both SiC and Si MOSFETs have a similar dV_{TH}/dT . The effective mobility (μ) also reduces with temperature as a result of increased phonon scattering reducing the relaxation time between carrier-to-lattice scattering events. The negative temperature coefficient of V_{TH} will reduce V_{GP} while the negative temperature coefficient of μ will increase V_{GP} . Hence, assuming a constant load current, the more dominant parameter will determine the temperature behaviour of V_{GP} with temperature. V_{GP} reduces with temperature in SiC MOSFETs while it is less temperature sensitive for Si MOSFETs.

Figure 3.18 (a) shows the V_{GS} turn-on transient for the 1200 V/20 A Si MOSFET with datasheet reference IXFX20N120P while Figure 3.18(b) shows the same measurements for a 1200 V/24 A SiC MOSFET from Cree/Wolfspeed with datasheet number CMF10120D. These measurements were performed with a low dI_{DS}/dt corresponding to an $R_G^{EXT}=220 \Omega$. In this figure, some of the characteristics that define the switching of SiC MOSFETs [8] compared to silicon MOSFETs are clearly identified:

- A higher value of the gate voltage plateau (V_{GP}) caused by a lower transconductance of the SiC MOSFETs
- A non-flat Miller plateau
- A significantly reduced transient duration for the gate voltage V_{GS} in the SiC MOSFETs as a result of the lower input capacitance

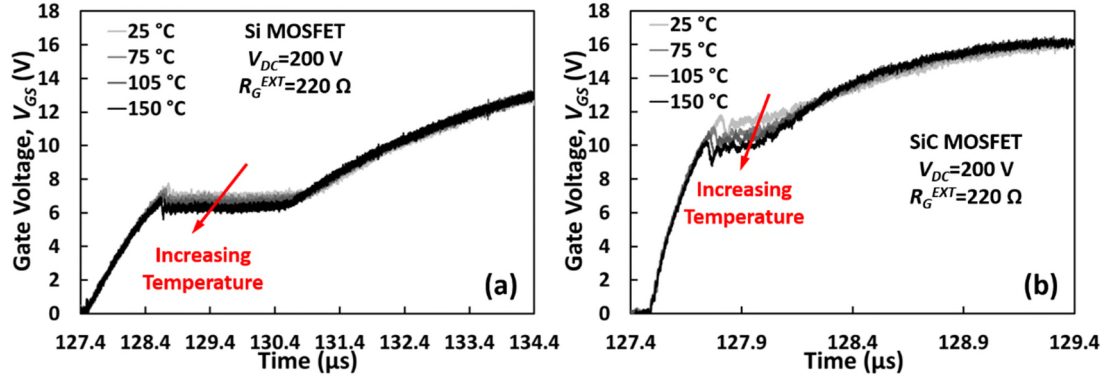


Figure 3.18 (a) V_{GS} turn-on transient for a Si MOSFET at different temperatures $R_G^{EXT}=220 \Omega$, (a) V_{GS} turn-on transient for a SiC MOSFET at different temperatures $R_G^{EXT}=220 \Omega$

It should be noted that at higher dI_{DS}/dt , the presence of parasitic inductance in the path of I_{DS} masks the changing behaviour of V_{GP} with temperature since the oscillations in I_G , V_{GS} and V_{DS} dominate the measured transient characteristics, as the measurements presented in Figure 3.19 show.

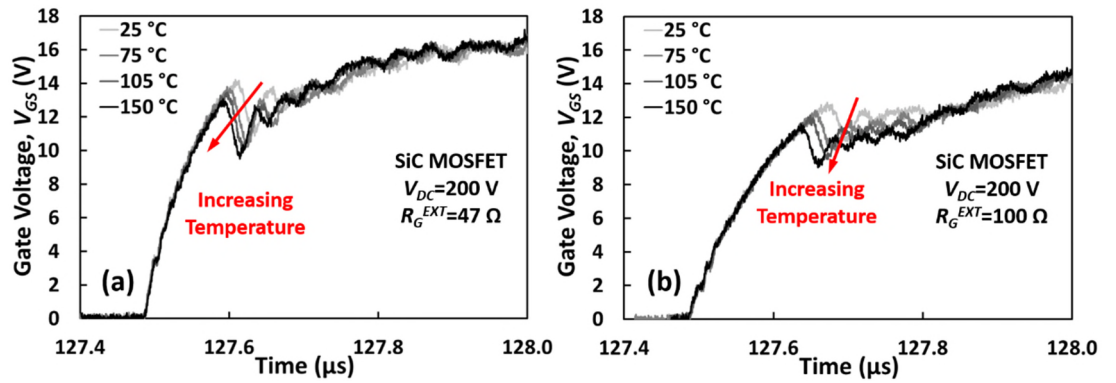


Figure 3.19 (a) V_{GS} turn-on transient for a SiC MOSFET at different temperatures $R_G^{EXT}=47 \Omega$, (a) V_{GS} turn-on transient for a SiC MOSFET at different temperatures $R_G^{EXT}=100 \Omega$

In the case of the SiC MOSFET the internal gate resistance has a considerably high value and an interesting observation is how the relationship between the external gate resistance and the internal gate resistance affects the value of the gate plateau, which

can be observed analysing Figure 3.20, where the turn-on transient of a SiC MOSFET using $R_G^{EXT}=47\ \Omega$ and $R_G^{EXT}=220\ \Omega$ is shown. The impact of the external gate resistance on the value of the plateau was already mentioned in [16] for IGBTs.

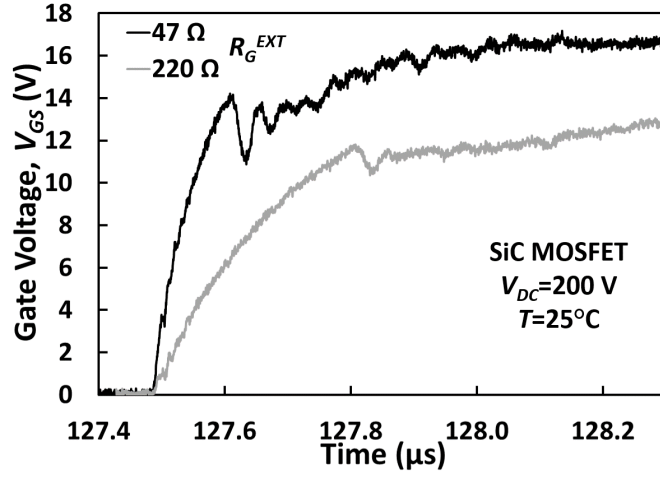


Figure 3.20 Impact of R_G^{EXT} on the gate plateau voltage during the turn-on transient

Referring back to Figure 3.17, between time t_l and t_2 , the Miller capacitance is charged and the V_{DS} transient occurs. At the end of t_2 , the V_{DS} transient is complete and the V_{GS} resumes its exponential rise to V_{GG} but with a larger time constant since the Miller capacitance has increased due to its dependency on the drain-source voltage V_{DS} . At higher temperatures, due to the lower threshold voltage, the turn-on transition times t_{TH}' , t_l' and t_2' are shifted in time as shown in Figure 3.17, indicating that the device turns on sooner.

Between time t_0 and t_l corresponding to the idealised switching transients shown in Figure 3.17, the gate voltage (V_{GS}) and its time derivative are given respectively by equation (3.7) and equation (3.8).

$$V_{GS} = V_{GG} \left(1 - e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT})C_{ISS}}} \right) \quad (3.7)$$

$$\frac{dV_{GS}}{dt} = \frac{V_{GG}}{(R_G^{INT} + R_G^{EXT})C_{ISS}} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT})C_{ISS}}} \quad (3.8)$$

When the gate voltage reaches the threshold voltage V_{TH} , the current starts to flow. Between time instants t_{TH} and t_l , assuming the MOSFET drain current is in saturation,

the drain-source current (I_{DS}) and its time derivative are given by equation (3.9) and equation (3.10) respectively, where β is the gain factor of the MOSFET.

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_{TH})^2 \quad (3.9)$$

$$\frac{dI_{DS}}{dt} = \beta (V_{GS} - V_{TH}) \frac{V_{GG}}{(R_G^{INT} + R_G^{EXT}) C_{ISS}} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT}) C_{ISS}}} \quad (3.10)$$

The temperature dependency of the current commutation rate (dI_{DS}/dt) during the turn-on transient can be calculated by taking the derivative of equation (3.10) with respect to temperature and is given by equation (3.11).

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{V_{GG} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT}) C_{ISS}}}}{(R_G^{INT} + R_G^{EXT}) C_{ISS}} \left(\beta \left| \frac{dV_{TH}}{dT} \right| - (V_{GS} - V_{TH}) \left| \frac{d\beta}{dT} \right| \right) \quad (3.11)$$

Given the temperature characteristics of different power MOSFETs, equation (3.11) could be used to identify the temperature sensitivity of the switching rate as a potential TSEP for condition monitoring. The turn-on transient for a series of silicon and silicon carbide devices, which are summarised in Table 3-I, has been measured using the double pulse test setup presented in chapter 2. The measurements were performed using a DC link voltage $V_{DC}=200$ V, a load current I_{DS} of 9 A, the gate driver voltage $V_{GG}=0/17$ V and external gate resistances R_G^{EXT} ranging from 10 Ω to 220 Ω .

Table 3-I: SiC and Si devices for evaluation of the temperature sensitivity of the current commutation rate during turn-on

Part Number	Description	Manufacturer
CMF10120D	1200 V/ 24 A SiC MOSFET 1 st Generation	Cree/Wolfspeed
CMF20120D	1200 V/ 42 A SiC MOSFET 1 st Generation	Cree/Wolfspeed
C2M0280120D	1200 V/ 10 A SiC MOSFET 2 nd Generation	Cree/Wolfspeed
C2M0160120D	1200 V/ 19 A SiC MOSFET 2 nd Generation	Cree/Wolfspeed
IGW15T120	1200 V/ 30 A Si IGBT	Infineon
IXFX20N120P	1200 V/ 20 A Si MOSFET	IXYS

Before the analysis of the switching rate it is convenient to summarise what has been presented previously in this thesis. In chapter 2 and in the introduction of this chapter the turn-on transient of the device current was characterised for different device technologies, at different temperatures and using different external gate resistances.

The switching rate as a function of the external gate resistance (R_G^{EXT}) at temperatures of 25 °C and 150 °C for the different devices evaluated is shown in Figure 3.21, where the switching rate was calculated as the average slope of the current for gate resistance values of 10, 47, 100 and 220 Ω .

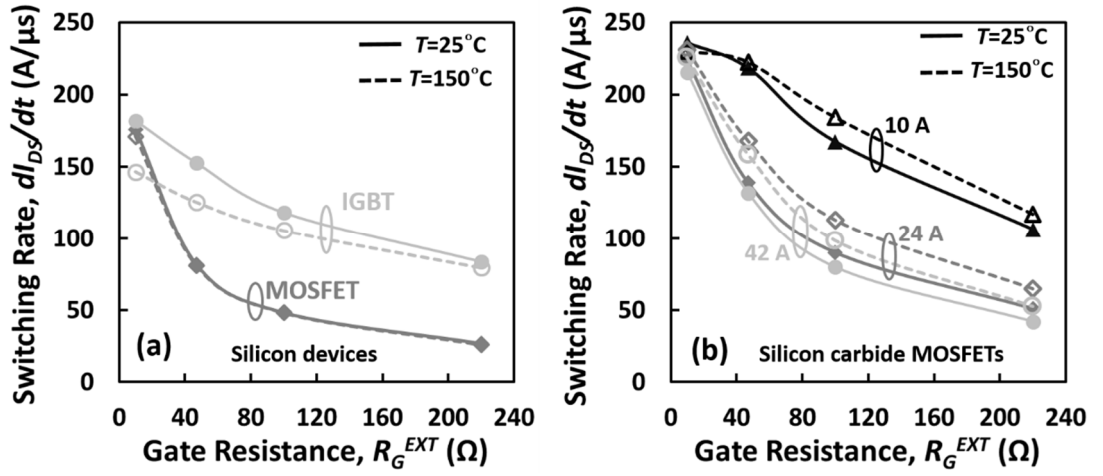


Figure 3.21 (a) Switching rate as a function of the external gate resistance (R_G^{EXT}) at temperatures of 25 °C and 150 °C: (a) Silicon devices (b) SiC MOSFETs

Figure 3.21(a) presents the measured switching rate for the evaluated silicon devices, namely a 1200 V MOSFET and a 1200 V IGBT. By comparing the switching rate measured at both temperatures, it can be seen that the switching rate of the silicon MOSFET can be considered temperature invariant while in the case of the IGBT the switching rate reduces with temperature, and the effect is more apparent when the devices are driven with a lower gate resistance, i.e. higher switching rates.

From the results presented in Figure 3.21(b), it can be observed that in the case of the evaluated SiC MOSFETs, the switching rate increases with temperature for all the evaluated devices. This increase is more evident when the device is switched using a large external gate resistance, hence at lower switching rates. From the presented measurements, it is also noticeable that the impact of temperature on the switching rate is higher for the higher current rated devices. This is clearly observed for the measurements performed using an external gate resistance R_G^{EXT} of 47 Ω .

Figure 3.22 presents the results of the three MOSFETs with similar rating: the first generation 1200 V/24 A SiC MOSFET and the second generation 1200 V/19 A SiC MOSFET from Cree/Woolfspeed, together with the 1200 V/20 A Si MOSFET from IXYS. In this figure it can be observed how the current commutation rate only reduces slightly for the Si MOSFET, while the turn-on dI_{DS}/dt increases with temperature for both SiC MOSFETs.

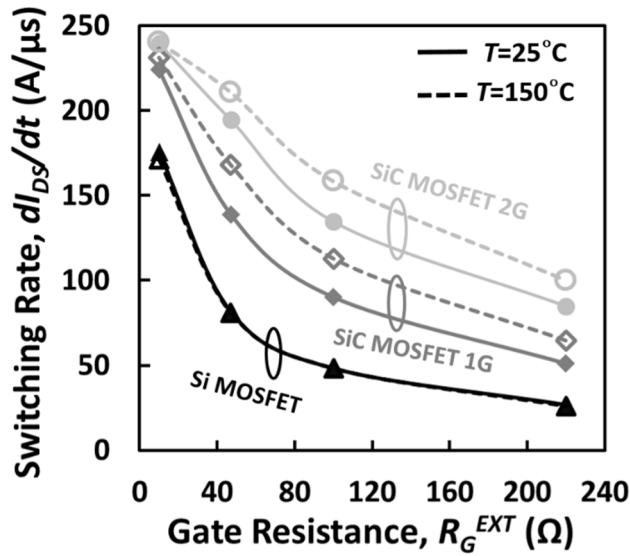


Figure 3.22 Switching rate as a function of the external gate resistance (R_{GEXT}) at temperatures of 25 °C and 150 °C for Si and SiC MOSFET of similar current rating

Analysing the results presented, it can be concluded that there are 3 factors affecting the switching rate of the device current and its temperature sensitivity, namely the device technology, the current rating and the external gate resistance. The following subsections evaluate the impact of this factors on the temperature sensitivity of the switching rate, together with the gate current characteristics.

The internal gate resistance and the gate current have been evaluated as TSEP in [17-20] with promising results. In this research it is analysed as a complementary indicator to the switching rate and its temperature sensitivity, given that the gate current is a good cursor of the turn-on transient.

3.3 Impact of device technology on dI_{DS}/dt as a TSEP

Equation (3.11) applies to all MOSFET technologies, however, the behaviour of dI_{DS}/dt with respect to temperature differs according to the device technology, as the measurements in Figure 3.21(b), and Figure 3.22 show.

Measurements from literature and datasheets show that for SiC MOSFETs, the turn-on dI_{DS}/dt increases with temperature [7, 14, 21], while for silicon MOSFETs devices [22], the turn-on dI_{DS}/dt is either temperature invariant or decreases with temperature. The reason for this is due to $d\beta/dT$, which is very low in SiC MOSFETs but is negative in silicon MOSFETs. β is dependent on temperature through the effective channel mobility which decreases as temperature increases but can be considered approximately constant for SiC MOSFETs due to its wide bandgap characteristics [23].

Figure 3.23 shows the turn-on drain-source (I_{DS}) transients for a 1200 V/24 A SiC MOSFET and a 1200 V/20 A Si MOSFET. The measurements were done using an external gate resistance R_G^{EXT} of 220 Ω . For both the silicon and silicon carbide MOSFETs, the drain current transient shifts leftwards in time as the temperature is increased due to the negative temperature coefficient of the threshold voltage causing the device to switch sooner at higher temperatures, as described in chapter 2, section 2.3.4. In the case of silicon MOSFETs, the dI_{DS}/dt does not increase with temperature so the current transients are approximately parallel, since the $d\beta/dT$ counteracts dV_{TH}/dT [22] thereby making dI_{DS}/dt less temperature sensitive, as the results in Figure 3.23(b) show. However, in SiC MOSFETs, $d\beta/dT$ can be neglected over the temperature range selected [23], hence dI_{DS}/dt increases with temperature due to dV_{TH}/dT , as Figure 3.23(a) shows.

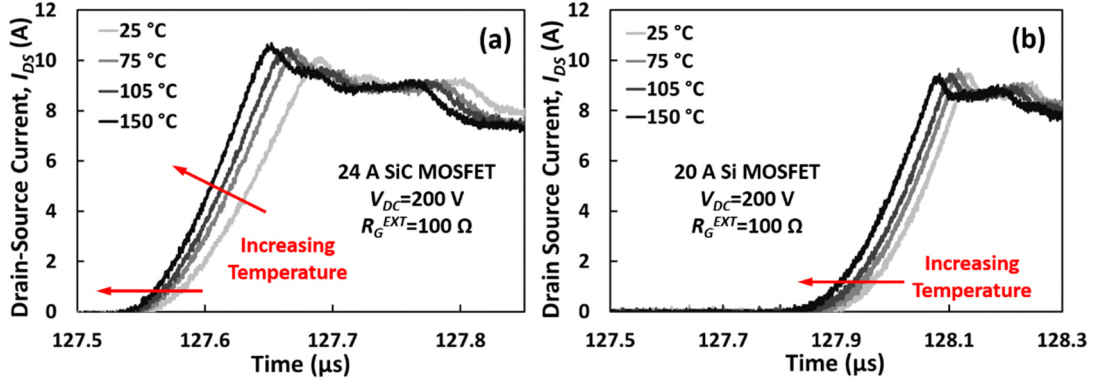


Figure 3.23 (a) Drain-source current (I_{DS}) for a 24 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=100 \Omega$, (b) Drain-source current (I_{DS}) for a 20 A Si MOSFET during turn-on at different temperatures, $R_G^{EXT}=100 \Omega$

The impact of temperature on the time shift of the turn-on transient (threshold voltage) was initially described in chapter 2, in section 2.3.4 and in the case of the evaluated silicon IGBT, the impact of the temperature on the turn-on delay is clearly observed if the device is slowed down, as it can be observed in Figure 3.24(b). However, the impact of temperature on the switching rate for the evaluated transient is more apparent when a lower external gate resistance is used.

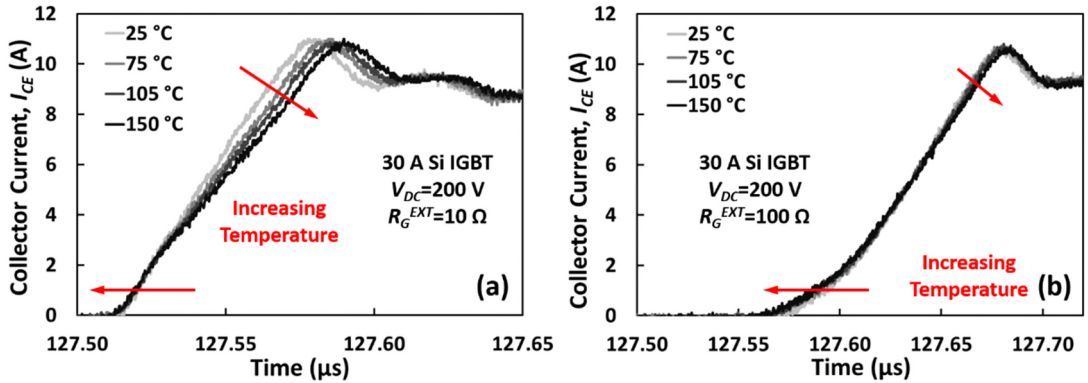


Figure 3.24 Collector-Emitter current (I_{CE}) for a 30 A Si IGBT during turn-on at different temperatures, $R_G^{EXT}=10 \Omega$, (b) Collector-Emitter current (I_{CE}) for a 30 A Si IGBT during turn-on at different temperatures, $R_G^{EXT}=100 \Omega$,

The switching rate of the collector current of the IGBT appears in this section for comparison purposes, as the switching rate is determined by a different equation than the MOSFET devices. According to [9, 24] for a fixed collector-emitter voltage the transconductance of an IGBT determines the relationship between the gate voltage and the collector current. The expression of the transconductance at pinch-off is given by equation (3.12).

$$\frac{dI_{CE}}{dt} \bigg/ \frac{dV_{GE}}{dt} = g_m = \frac{1}{1 - \alpha_{pnp}} \left(\mu_{ni} C_{OX} \frac{W}{L} (V_{GE} - V_{TH}) \right) \quad (3.12)$$

The first term of equation (3.12) represents the contribution of the inherent bipolar transistor, with the temperature dependency given by the gain α_{pnp} and the second term represents MOSFET part contribution, with the mobility μ and threshold voltage V_{TH} affected by temperature. C_{OX} is the gate oxide capacitance density, W is the width of the channel is, L is the length of the channel and V_{GE} is the gate-emitter voltage. This causes the turn-on transient of the current of an IGBT to have a characteristic double temperature coefficient.

As it was previously presented in section 3.2, the gate current can be used as a cursor of the turn-on transient. Figure 3.25 shows the gate current during turn-on for the 24 A SiC MOSFET and the 20 A Si MOSFET, where it is clearly observed how the impact of temperature on the gate current plateau value for the SiC MOSFET is higher than for the silicon MOSFET.

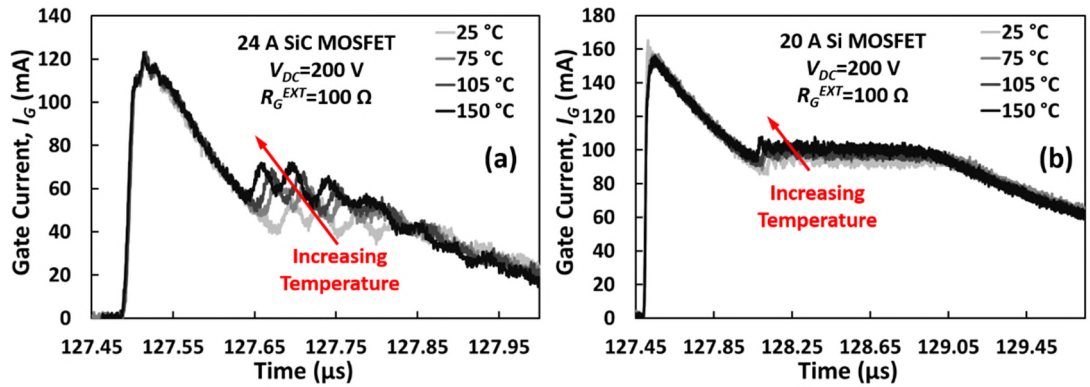


Figure 3.25 (a) Gate current (I_G) for a 24 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=100$ Ω (b) Gate current (I_G) for a 20 A Si MOSFET during turn-on at different temperatures, $R_G^{EXT}=100$ Ω

The internal gate resistance is lower for the silicon MOSFET, which causes the peak gate current to be higher for the silicon MOSFET. The impact of the parasitic capacitances of the MOSFET on the turn-on transient is clearly identified by comparing Figure 3.25(a) and Figure 3.25(b), with a longer transient duration and a defined and longer gate current plateau in the case of the silicon MOSFET.

In the case of the evaluated IGBT, the gate current transient during turn-on is presented in Figure 3.26. According to these measurements, for the evaluated IGBT there is no apparent temperature sensitivity of the gate current plateau, compared with the MOSFET devices. However what is observed is a slight temperature sensitivity on the time to plateau, with is more apparent for a smaller gate resistance, as the results in Figure 3.26(a) show.

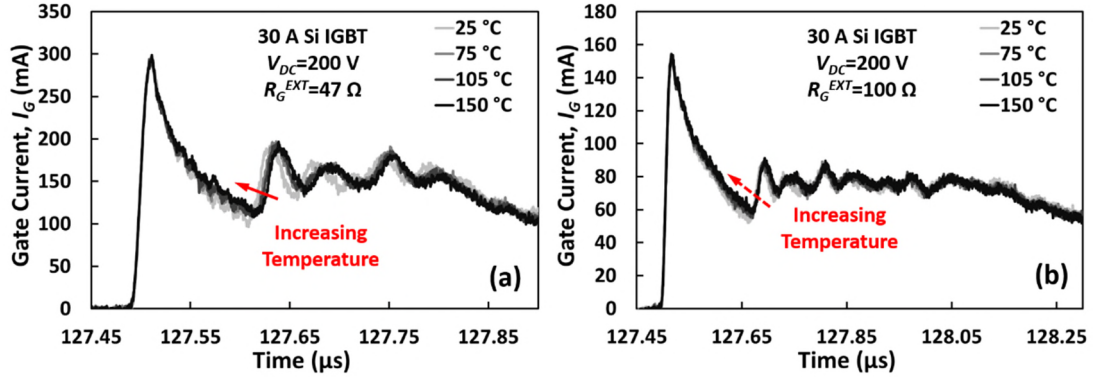


Figure 3.26 (a) Gate current (I_G) for a 30 A Si IGBT during turn-on at different temperatures, (a) $R_G^{EXT}=47\ \Omega$ (b) $R_G^{EXT}=100\ \Omega$

3.4 Impact of device current rating on dI_{DS}/dt as TSEP

The turn-on current commutation rate of the SiC MOSFET has been identified as a potential TSEP. However, the temperature sensitivity of dI_{DS}/dt in SiC power MOSFETs needs to be investigated as a function of the device current rating.

Figure 3.27 shows the drain-source and gate current transient during turn-on for a 1200 V/10 A SiC MOSFET while Figure 3.28 shows the measurements for the 1200 V/42 A SiC MOSFET. For both devices the external gate resistance used is 220 Ω . It can be seen by comparing Figure 3.27(a) and Figure 3.28 (b), that the temperature sensitivity of dI_{DS}/dt is smaller for the 10 A SiC MOSFET compared to the 42 A SiC MOSFET. The temperature sensitivity of the gate current plateau (I_{GP}) is also higher for the 42 A MOSFET.

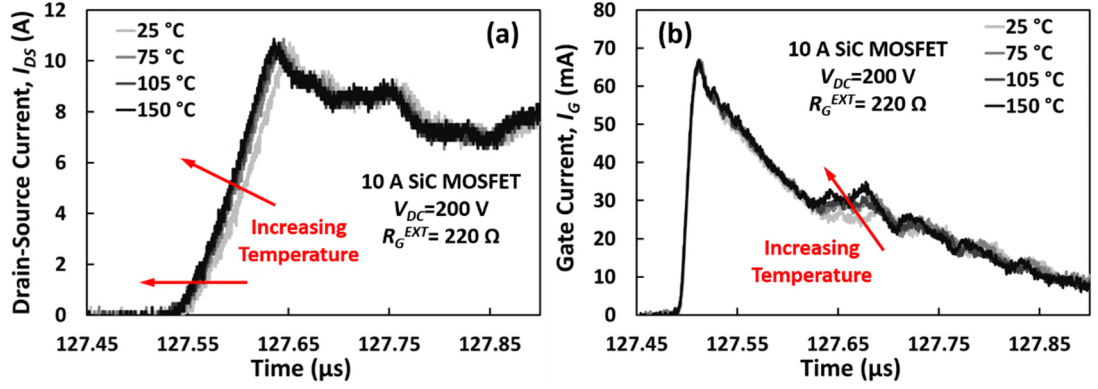


Figure 3.27 (a) Drain-source current (I_{DS}) for a 10 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=220 \Omega$ (b) Gate current (I_G) for a 10 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=220 \Omega$

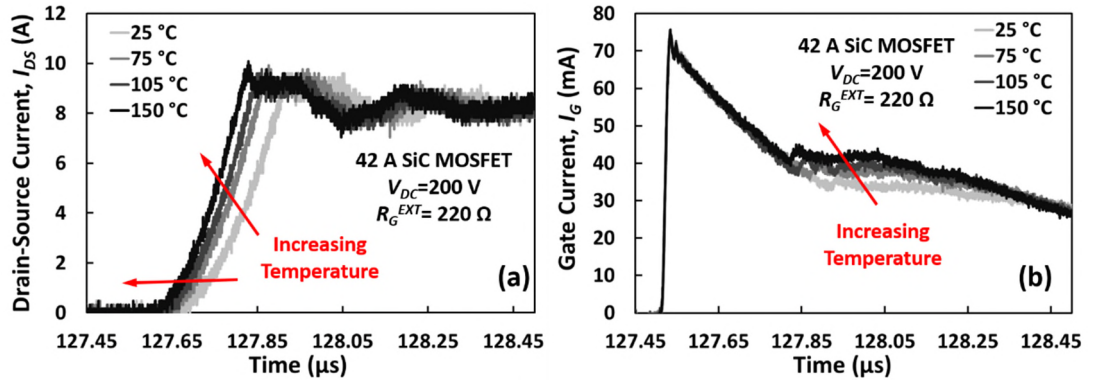


Figure 3.28 (a) Drain-source current (I_{DS}) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=220 \Omega$ (b) Gate current (I_G) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT}=220 \Omega$

Due to the fact that the 10 A die is physically smaller compared to the 42 A die, it has a smaller switching time constant which can be expressed as the product of the total input resistance and the total input capacitance i.e. $(R_G^{EXT}+R_G^{INT})C_{ISS}$. The 10 A SiC MOSFET has an input capacitance of 0.259 nF according to its datasheet, while the input capacitance is 1.915 nF for the 42 A device. The result is significantly higher dI_{DS}/dt in the 10 A MOSFET compared to the 42 A SiC MOSFET when both devices are driven using the same external gate resistance, as it was shown in Figure 3.21(b).

A large external gate resistance of 220Ω was used in these measurements, partially to limit the impact of the internal gate resistance (which is 5Ω for the 42 A SiC MOSFET and 11.4Ω for the 10 A device) and to improve the time resolution of the gate current plateau, as it can be observed in Figure 3.27(a) and Figure 3.28(b). It is also important to mention that the smaller devices have lower parasitic capacitances, affecting the time duration of the different stages of the gate current. This is clearly noticeable

evaluating the duration of the gate current plateau for both devices, as shown in Figure 3.27(a) and Figure 3.28(b).

Large gate resistances were used to exaggerate the transient duration, however, in practical applications where there is a need to minimise switching losses and expedite the fast switching potential of SiC MOSFETs, a smaller gate resistance is preferable. Measurements of the drain-source current and the gate current turn-on transients using external gate resistances of $10\ \Omega$ and $47\ \Omega$ have been performed for the 10 A and 42 A SiC MOSFETs. The captured transients are shown in Figure 3.29 to Figure 3.32.

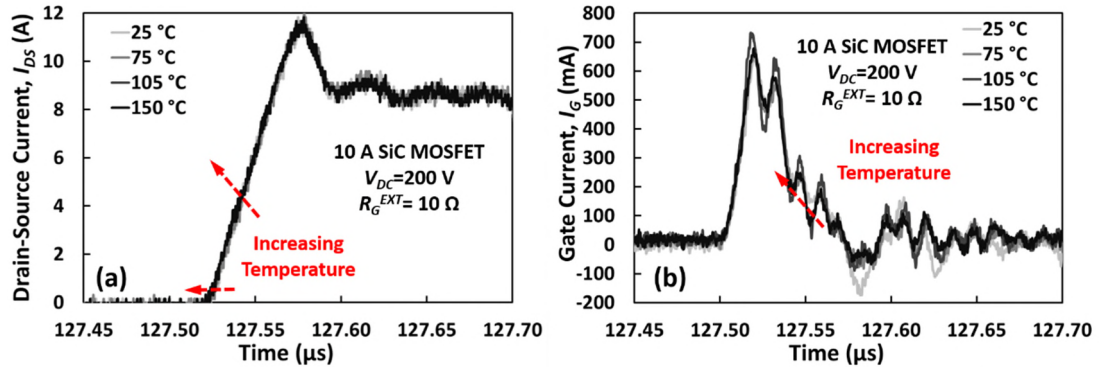


Figure 3.29 (a) Drain-source current (I_{DS}) for a 10 A SiC MOSFET during turn-on at different temperatures, (b) Gate current (I_G) for a 10 A SiC MOSFET during turn-on at different temperatures

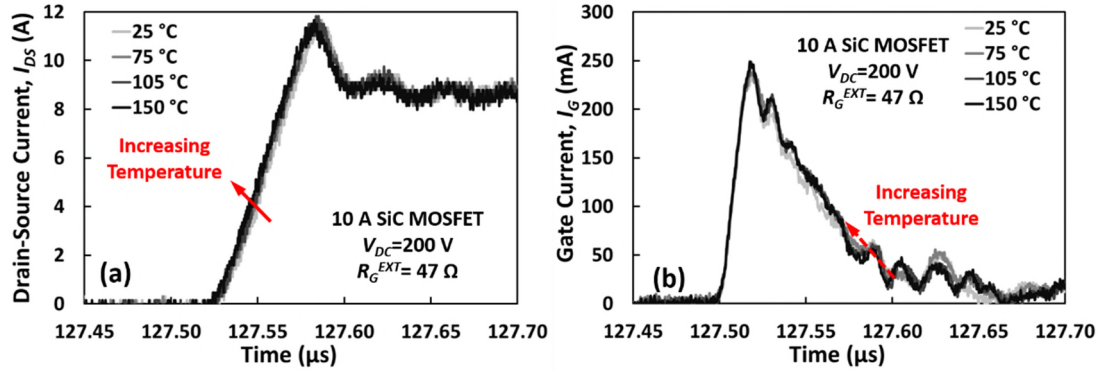


Figure 3.30 (a) Drain-source current (I_{DS}) for a 10 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 47\ \Omega$ (b) Gate current (I_G) for a 10 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 47\ \Omega$

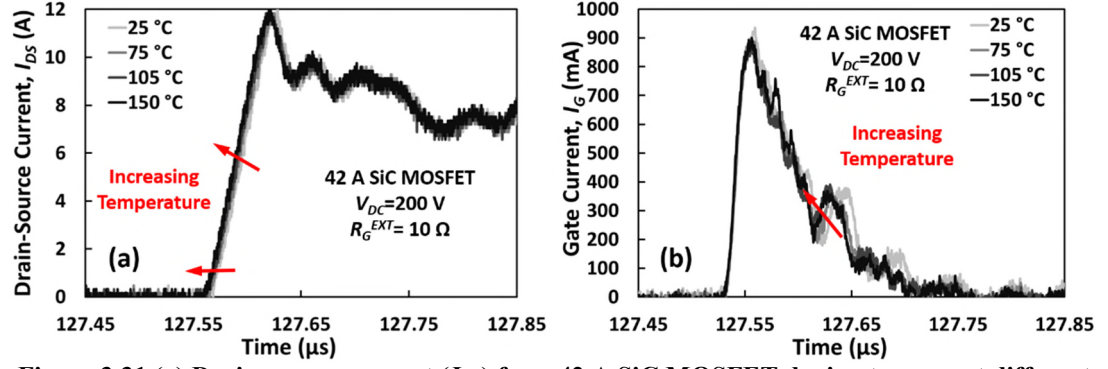


Figure 3.31 (a) Drain-source current (I_{DS}) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 10 \Omega$ (b) Gate current (I_G) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 10 \Omega$

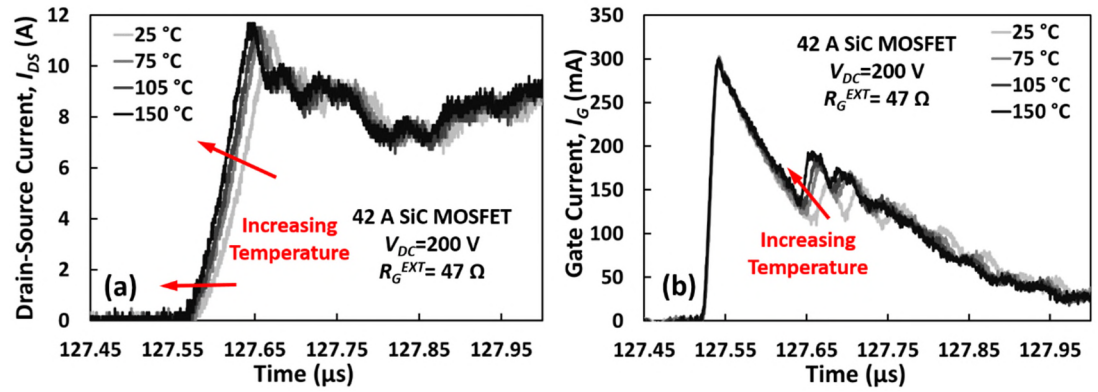


Figure 3.32 (a) Drain-source current (I_{DS}) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 47 \Omega$ (b) Gate current (I_G) for a 42 A SiC MOSFET during turn-on at different temperatures, $R_G^{EXT} = 47 \Omega$

Analysing the waveforms presented in Figure 3.29 to Figure 3.32 it is clearly observed that the temperature sensitivity of the turn-on transient is more apparent for the device with a higher current rating. This can be observed in the increase of dI_{DS}/dt and the device turning on sooner in time. This is caused by the higher parasitic capacitances, which result in a higher time constant when the MOSFETs are driven with the same external gate resistance. The impact of a higher Miller capacitance in the gate current transient is specially clear for the 42 A SiC MOSFET, causing a more defined gate current plateau compared with the 10 A SiC MOSFET. It can also be seen from Figure 3.29 and Figure 3.31 that at low R_G^{EXT} , the temperature sensitivity of dI_{DS}/dt reduces for both SiC MOSFETs.

As will be shown in the next section, reducing the external gate resistance, hence a higher nominal switching rate, increases the impact of the parasitic inductance which affects the effectiveness of dI_{DS}/dt as a TSEP in SiC MOSFETs.

3.5 Impact of the external gate resistance R_G^{EXT} on dI_{DS}/dt as TSEP

In section 3.4 it was shown how reducing the nominal switching rate by means of increasing the external gate resistance improved the temperature sensitivity of dI_{DS}/dt . In this section of this chapter, the effectiveness of the turn-on dI_{DS}/dt as a TSEP in SiC MOSFETs is investigated over a range of external gate resistance for devices of different current ratings, namely the 10 A, 19 A, 24 A and 42 A SiC MOSFETs, as described in Table 3-I. The turn-on transients were captured using the experimental setup described in chapter 2. The turn-on transients for the 19 A and 24 A SiC MOSFETs are shown in Figure 3.33 and Figure 3.34, using external gate resistance values of 10, 47, 100 and 220 Ω . Different turn-on transients for the 10 A and 42 A SiC MOSFETs have been already shown in previous sections of this chapter.

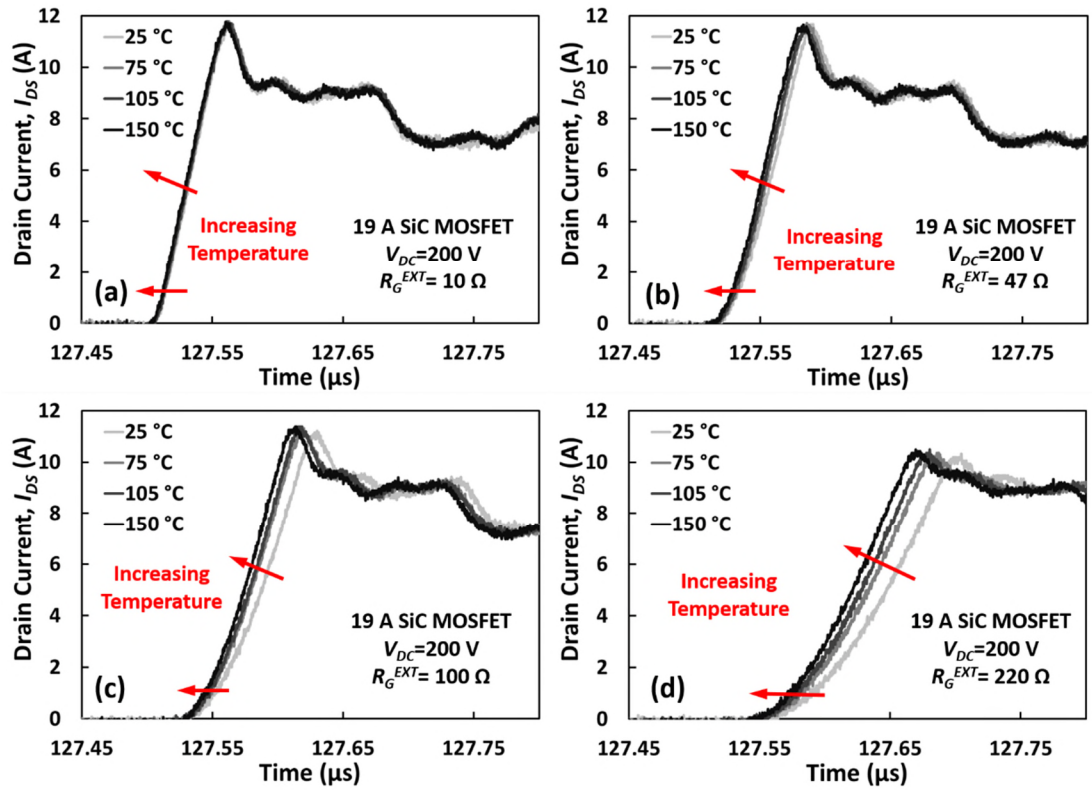


Figure 3.33 Drain-source current (I_{DS}) for a 19 A SiC MOSFET during turn-on at different temperatures: (a) $R_G^{EXT}=10$ Ω , (b) $R_G^{EXT}=47$ Ω , (c) $R_G^{EXT}=100$ Ω , (d) $R_G^{EXT}=220$ Ω

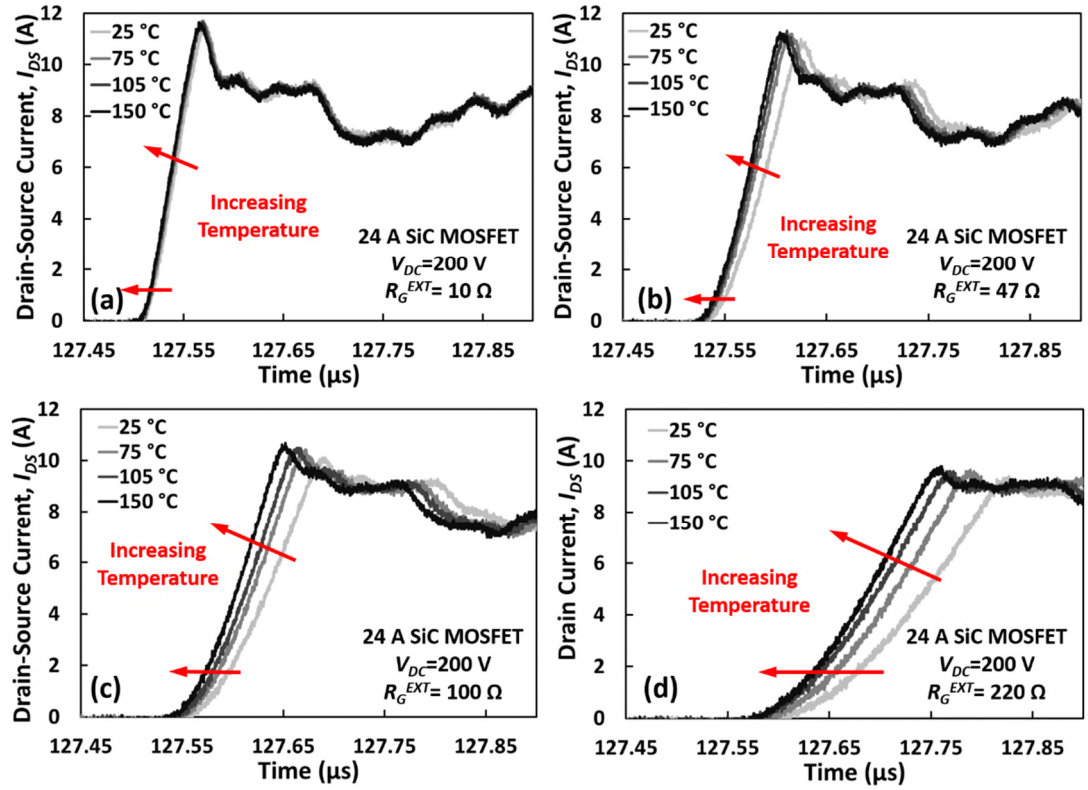


Figure 3.34 Drain-source current (I_{DS}) for a 24 A SiC MOSFET during turn-on at different temperatures: (a) $R_G^{EXT}=10\ \Omega$, (b) $R_G^{EXT}=47\ \Omega$, (c) $R_G^{EXT}=100\ \Omega$, (d) $R_G^{EXT}=220\ \Omega$

The dI_{DS}/dt was calculated as the slope of the linear regression of the drain current for the 4 SiC MOSFETs and the results are summarised in Table 3-II.

Table 3-II: Switching rate during turn-on for the evaluated 1200 V SiC MOSFETs at different temperatures and external gate resistances

	10 A SiC MOSFET (C2M0280120D)				19 A SiC MOSFET (C2M160120D)			
$(R_G^{INT}+R_G^{EXT})C_{ISS}$ (ns)	5.5	15.1	28.9	59.9	8.7	28.1	55.9	118.9
$dI_{DS}/dt, T=25\ ^\circ\text{C}$ (A/ μs)	235.8	218.3	167.3	106.6	239.6	194.4	134.6	84.8
$dI_{DS}/dt, T=75\ ^\circ\text{C}$ (A/ μs)	234.0	222.1	173.8	112.1	241.5	205.2	146.8	93.0
$dI_{DS}/dt, T=105\ ^\circ\text{C}$ (A/ μs)	231.6	227.2	179.5	116.6	240.1	204.8	151.3	95.8
$dI_{DS}/dt, T=150\ ^\circ\text{C}$ (A/ μs)	229.9	222.3	184.1	116.9	240.1	210.6	158.3	100.1
	24 A SiC MOSFET (CMF10120D)				42 A SiC MOSFET (CMF20120D)			
$(R_G^{INT}+R_G^{EXT})C_{ISS}$ (ns)	21.9	56.2	105.4	216.8	28.7	99.6	201.1	430.9
$dI_{DS}/dt, T=25\ ^\circ\text{C}$ (A/ μs)	223.9	138.9	90.1	51.1	215.5	132.0	80.0	42.1
$dI_{DS}/dt, T=75\ ^\circ\text{C}$ (A/ μs)	228.8	153.7	101.3	57.6	219.7	145.1	88.9	47.0
$dI_{DS}/dt, T=105\ ^\circ\text{C}$ (A/ μs)	229.9	161.2	106.3	60.7	224.0	151.6	92.5	49.7
$dI_{DS}/dt, T=150\ ^\circ\text{C}$ (A/ μs)	231.2	168.0	112.9	64.6	225.4	158.4	98.4	52.4

In Table 3-II the switching time constant, which is given by $(R_G^{EXT} + R_G^{INT})C_{ISS}$, is used to compare the switching rates of the different devices, with different internal gate resistances and input capacitances, as shown in Table 3-III.

Table 3-III Internal gate resistance and input capacitance of the evaluated SiC MOSFETs

Part Number	Internal Gate Resistance R_G^{INT} (Ω)	Input capacitance C_{ISS} (pF)
CMF10120D	13.6	928
CMF20120D	5	1915
C2M0280120D	11.4	259
C2M0160120D	6.5	525

The values presented in Table 3-II are plotted in Figure 3.35 and Figure 3.36. Figure 3.35(a) shows the switching rate as a function of the RC constant for the 10 A and 19 A SiC MOSFETs at a temperature of 25 °C, while Figure 3.35(b) presents the switching rate at a temperature of 150 °C. Figure 3.36(a) and Figure 3.36(b) present the switching rate for the 24 A and 42 A SiC MOSFETs at 25 °C and 150 °C respectively.

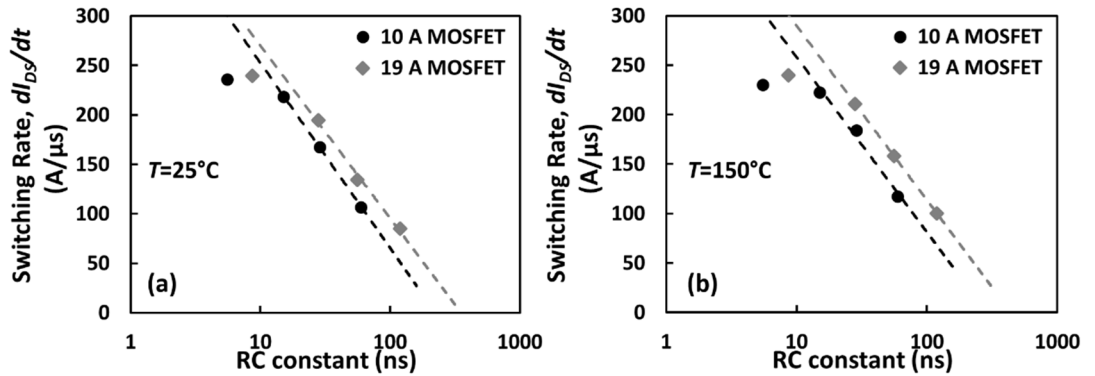


Figure 3.35 Measured turn-on dI_{DS}/dt as a function of the RC constant for the 10 and 19 A SiC MOSFETs (a) 25 °C (b) 150 °C

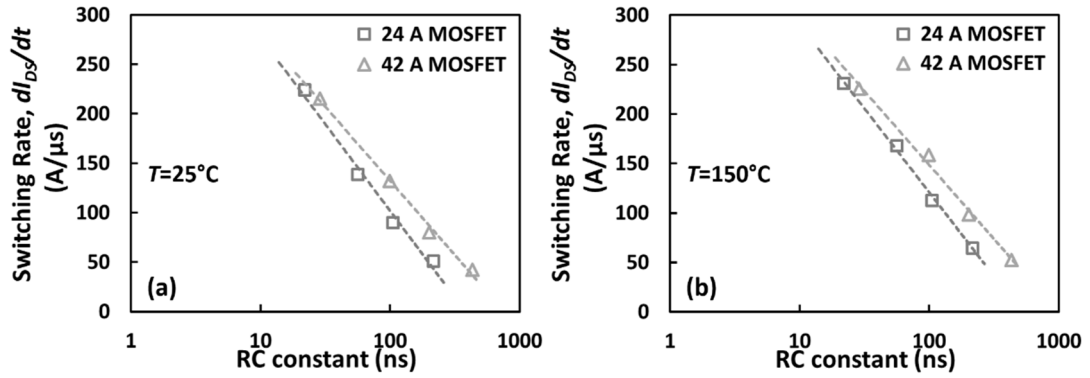


Figure 3.36 Measured turn-on dI_{DS}/dt as a function of the RC constant for the 24 and 42 A SiC MOSFETs (a) 25 °C (b) 150 °C

It can be observed that the 4 devices have similar maximum switching rates for the smaller RC constants, but in the case of the 10 A and 19 A SiC MOSFET, the dI_{DS}/dt is clearly limited by the impact of the inductance on the load path. These two MOSFETs are second generation devices, with lower input capacitances, compared with the first generation devices, hence they switch faster if the same external gate resistance is used.

Both figures showed that the MOSFETs with a higher transconductance will exhibit a higher switching rate compared to a MOSFET with a lower transconductance if both are switched with the same RC time constant. Hence, in Figure 3.36 the 42 A MOSFET switches with the highest switching rate because the transconductance increases with the current rating through increased chip area.

The normalised dI_{DS}/dt as a function of temperature for different external gate resistances (R_G^{EXT}) for the evaluated SiC MOSFETs is shown in Figure 3.37. The results presented in this figure generally show that the temperature sensitivity of dI_{DS}/dt decreases with the external gate resistance as well as with the current rating i.e. to use dI_{DS}/dt as a TSEP, the SiC MOSFET must be driven with a large external gate resistance and the technique would be most effective when the device current rating is high.

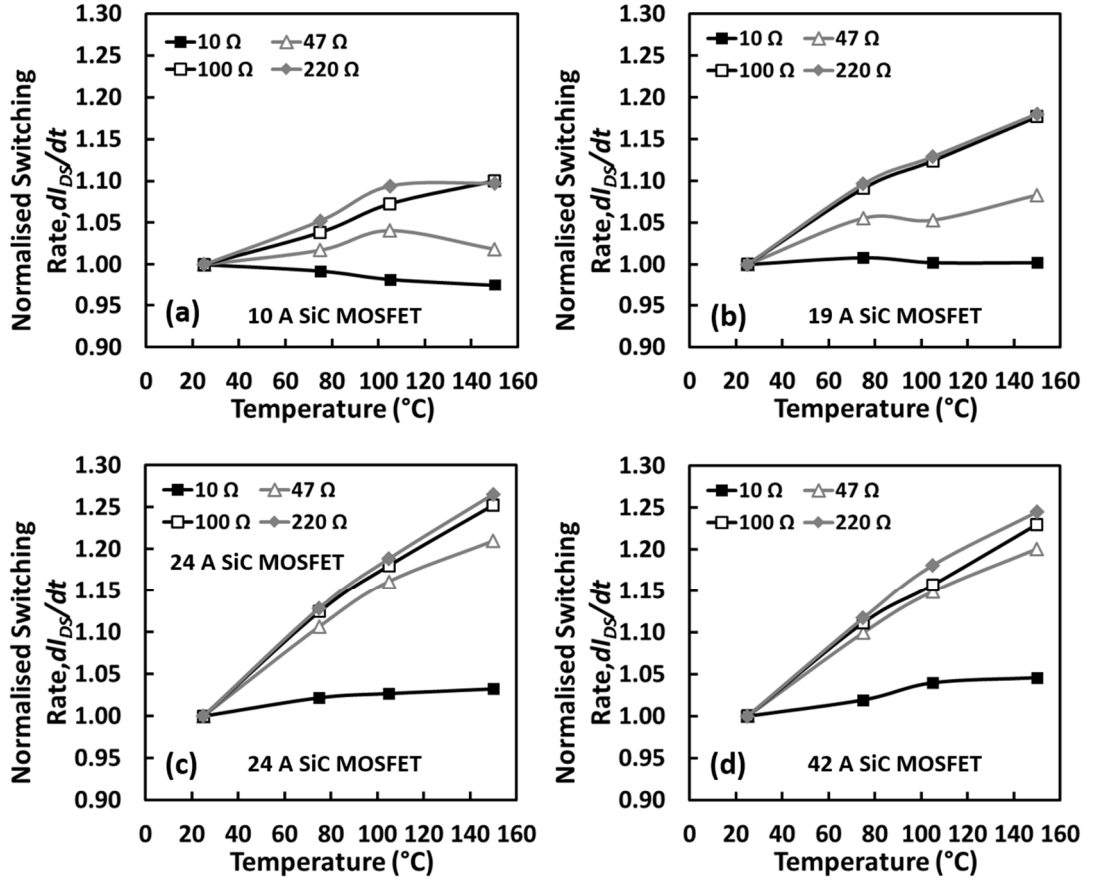


Figure 3.37 Normalised dI_{DS}/dt as a function of temperature for different R_G^{EXT} : (a) 10 A SiC MOSFET, (b) 19 A SiC MOSFET, (c) 24 A SiC MOSFET, (d) 42 A SiC MOSFET

Figure 3.38(a) to Figure 3.38(d) show the gate current measurements for the 42 A SiC MOSFET using gate resistances R_G^{EXT} of 10, 47, 100 and 220 Ω respectively. From the results presented in this figure it can be seen that the temperature dependency of the gate current plateau is higher for the large external gate resistances (47 to 220 Ω) and the impact of the oscillations has also been minimised. This is clearly observed in Figure 3.38(d), where a $R_G^{EXT}=220\ \Omega$ is used, with a more defined plateau and reduced oscillations of the gate current transient. The temperature sensitivity of time to plateau $t_{plateau}$ benefits from increasing the external gate resistance, with a variation of the time to plateau $\Delta t_{plateau}$ between temperatures of 25 °C and 150 °C of 105 ns. This clearly indicates that the gate current and its plateau are a TSEP more suitable for higher current rating devices, switched with a large external gate resistance. However, the variation of the gate current plateau ΔI_{GP} and its time transients as TSEP have a significant trade-off which will be analysed in section 3.6.

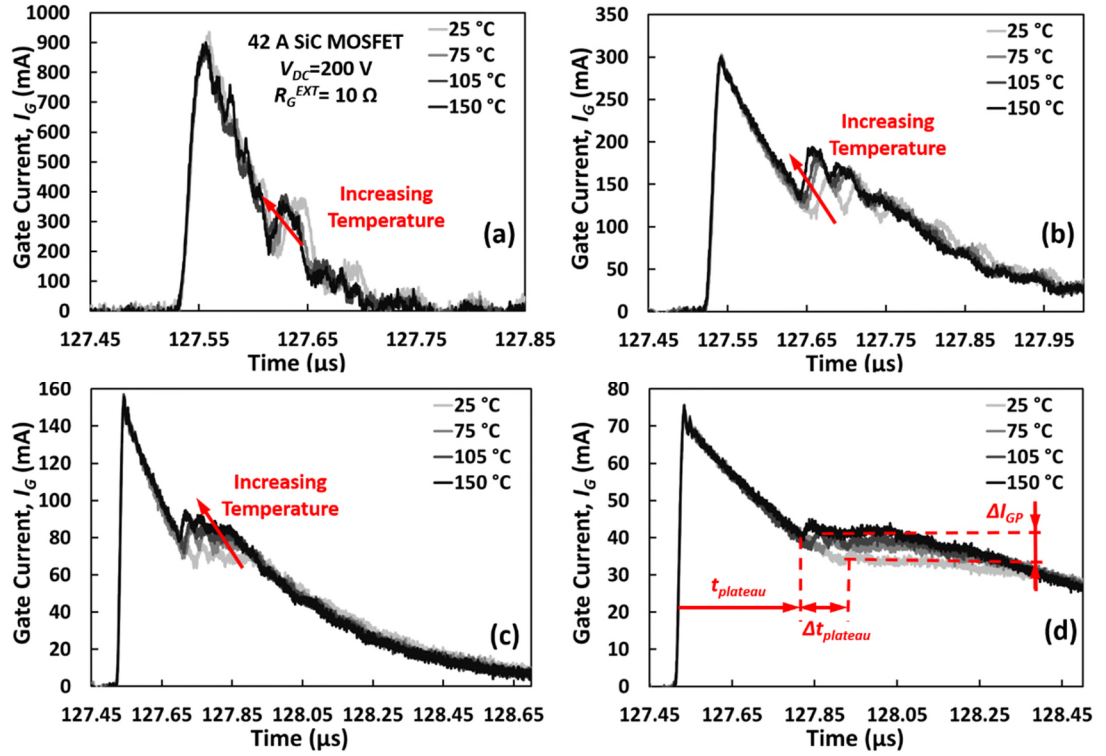


Figure 3.38 Gate current (I_G) for a 42 A SiC MOSFET during turn-on at different temperatures:
 (a) $R_G^{EXT}=10 \Omega$, (b) $R_G^{EXT}=47 \Omega$, (c) $R_G^{EXT}=100 \Omega$, (d) $R_G^{EXT}=220 \Omega$

Equations (3.13) and (3.14) model the turn-on I_{DS} for the MOSFET and its time derivative respectively. However, the presence of the source inductance means that the source voltage can no longer be assumed to be zero but instead is given as the product of the source inductance and the dI_{DS}/dt . To understand the reduction of temperature sensitivity of dI_{DS}/dt at small R_G^{EXT} and at smaller current ratings (i.e. faster switching rates), it is important to re-derive the equations of dI_{DS}/dt and its temperature sensitivity adding the effect of the parasitic source inductance (L_S) [25, 26].

$$I_{DS} = \frac{\beta}{2} (V_G - V_S - V_{TH})^2 \quad \text{where } V_S = L_S \frac{dI_{DS}}{dt} \quad (3.13)$$

$$\frac{dI_{DS}}{dt} = \beta \left(V_G - L_S \frac{dI_{DS}}{dt} - V_{TH} \right) \left(\frac{dV_G}{dt} - L_S \frac{d^2 I_{DS}}{dt^2} \right) \quad (3.14)$$

Equation (3.14) is a 2nd order ordinary differential equation (ODE) which can be simplified by assuming a constant dI_{DS}/dt whose derivative ($d^2 I_{DS}/dt^2$) is therefore zero.

This assumption does not reduce the accuracy of the proposed model as will be seen later. Hence, the turn-on dI_{DS}/dt can be expressed using equation (3.15).

$$\frac{dI_{DS}}{dt} = \frac{\beta(V_G - V_{TH}) \left(\frac{dV_G}{dt} \right)}{1 + \beta L_S \left(\frac{dV_G}{dt} \right)} \quad (3.15)$$

When equation (3.15) is combined with equation (3.8), the resultant equation is

$$\frac{dI_{DS}}{dt} = \frac{\beta(V_G - V_{TH}) \left(\frac{V_{GG}}{(R_G^{INT} + R_G^{EXT})(C_{ISS})} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT})(C_{ISS})}} \right)}{1 + \beta L_S \left(\frac{V_{GG}}{(R_G^{INT} + R_G^{EXT})(C_{ISS})} e^{-\frac{t-t_0}{(R_G^{INT} + R_G^{EXT})(C_{ISS})}} \right)} \quad (3.16)$$

Equation (3.16) is useful for understanding how the current commutation rate is determined by the external gate resistance and temperature in the presence of parasitic inductance in the source-drain current path. It is well understood that reducing the R_G^{EXT} increases dI_{DS}/dt , however, the rate at which this occurs also depends on the parasitic capacitances, the internal gate resistance, the parasitic inductance and temperature.

Using (3.16), dI_{DS}/dt has been calculated for the 1.2kV/42 A SiC MOSFETs for different external gate resistances, temperatures and parasitic inductances. The dI_{DS}/dt has been calculated for a load current I_{DS} of 9 A and assuming a constant mobility for the SiC MOSFET as has been discussed in section 3.3. Datasheet parameters were used in equation (3.16), including $C_{ISS}=1.915$ nF, internal gate resistance $R_G^{INT}=5$ Ω and a threshold voltage of 3.2 V at 25 °C and 2.3 V at 150 °C. The gate drive voltage used was $V_{GG}=18$ V.

Figure 3.39(a) shows the results of the model for different R_G^{EXT} and parasitic inductance together with experimental measurements at 25 °C while Figure 3.39(b) shows similar modelling and measurement results at 150 °C. It can be seen that the model and measurements agree when a large R_G^{EXT} is used, however, as R_G^{EXT} is reduced and dI_{DS}/dt is increased, the model matches the measurements when parasitic inductance is accounted for. The model shows that the parasitic inductance is within the range of 15 to 20 nH. By

comparing the modelled and measured dI_{DS}/dt at the different temperatures for the different R_G^{EXT} , it was observed that the positive temperature coefficient of dI_{DS}/dt reduced with decreasing R_G^{EXT} as a result of the parasitic inductance. And this effect was more apparent at high dI_{DS}/dt which explains why the 10 A SiC MOSFET (with significantly reduced input capacitance) exhibited a dI_{DS}/dt that was temperature insensitive at low R_G^{EXT} .

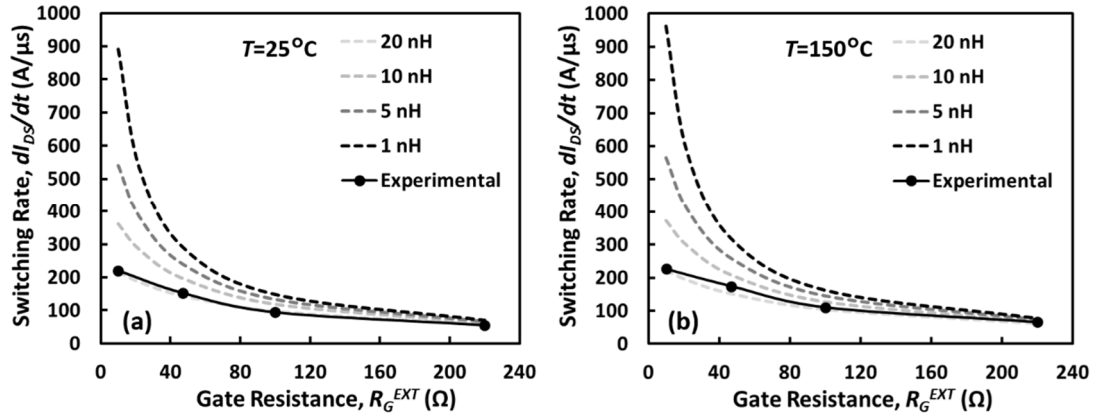


Figure 3.39 (a) Modelled and measured turn-on dI_{DS}/dt for the 42 A SiC MOSFET showing the impact of parasitic inductance, $T=25^\circ\text{C}$, (b) Modelled and measured turn-on dI_{DS}/dt for the 42 A SiC MOSFET showing the impact of parasitic inductance, $T=150^\circ\text{C}$

Hence, this shows that the parasitic inductance (i.e. the packaging) reduces the temperature sensitivity of dI_{DS}/dt . It is important to mention that the impact of the parasitic inductance L_S not only limits the temperature sensitivity of dI_{DS}/dt as shown previously in this chapter, but it can also be used as a temperature sensor if there is an additional terminal connected to the internal source of the power module, meaning that the voltage drop across the parasitic inductance can be measured. This method of using auxiliary terminals across the stray inductance has been proposed for identifying the turn-off delay in IGBTs [6]. Equation (3.13) suggests that the voltage across the stray inductance can be used for identifying dI_{DS}/dt and junction temperatures in SiC MOSFETs.

3.6 Results for condition monitoring implementation

The use of the switching rate as TSEP for condition monitoring in SiC power MOSFETs requires to understand and calibrate its relationship with other parameters like load current and DC link voltage. Any load current and/or voltage dependency of dI_{DS}/dt should be decoupled from its temperature dependency so that it can be used for junction temperature sensing.

The measurements and analysis presented previously in this chapter were performed using a DC link voltage of 200 V which is well below the 1200 V rated blocking voltage of the SiC MOSFETs studied. From the application point of view, in applications like automotive drivetrains [27] DC link voltages of 300 to 600 V are widely used, hence the evaluation of dI_{DS}/dt and its temperature sensitivity at those voltage levels should be investigated.

The dependency of the switching rate on the DC link voltage and temperature has been investigated by a set of experimental measurements using the double pulse test configuration which has been used throughout this chapter, adjusting the DC link voltage value. The turn-on transient of the 42 A SiC MOSFET was characterised for different DC link voltages, using an external gate resistance R_G^{EXT} of 220 Ω . The evaluated DC link voltage values (V_{DC}) are 75 V, 150 V, 300 V and 600 V. The turn-on transients of I_{DS} , measured at temperatures of 25 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$, are shown in Figure 3.40(a) and Figure 3.40(b) respectively.

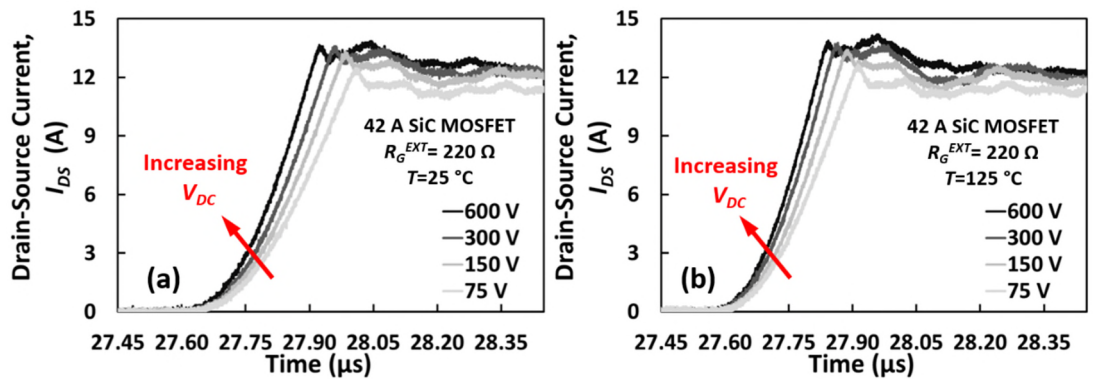


Figure 3.40 (a) Drain-Source current (I_{DS}) for the 42 A SiC MOSFET during turn-on for different DC link voltages. $R_G^{EXT}=220\ \Omega$ and $T=25\ ^{\circ}\text{C}$, (b) Drain-Source current (I_{DS}) for the 42 A SiC MOSFET during turn-on for different DC link voltages. $R_G^{EXT}=220\ \Omega$ and $T=125\ ^{\circ}\text{C}$

From the results presented in Figure 3.40, it can be observed that the turn-on switching rate is increasing with the supply voltage. This is due to the fact that the input capacitance reduces with increasing DC supply voltage as a result of the voltage-dependent Miller capacitance. The Miller capacitance is comprised of a series combination of an oxide capacitance and a voltage dependent depletion capacitance that increases as the supply voltage reduces. Increasing the supply voltage increases the depletion width and hence reduces the Miller capacitance [12]. Hence, at low V_{DC} , the high Miller capacitance slows down the MOSFET. Since in voltage source converter applications the DC link voltage is usually held constant, the dependency of dI_{DS}/dt on V_{DC} is not critical in its use as a TSEP.

The measurements presented on Figure 3.40 were performed at two temperatures, namely 25 °C and 125 °C. The turn-on transients for a DC link voltage of 600 V are presented in Figure 3.41(a), where it can be observed that the switching rate increases with temperature, together with a shift in time.

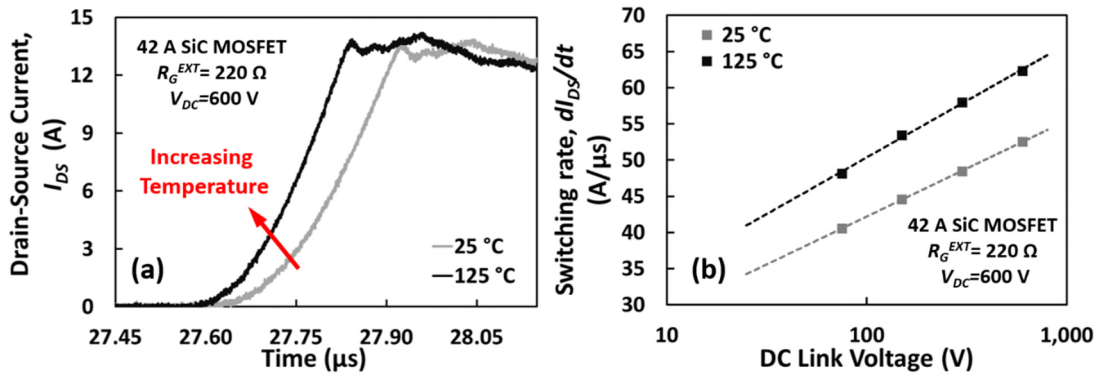


Figure 3.41 (a) Drain-Source current (I_{DS}) for the 42 A SiC MOSFET during turn-on for different at $T=25$ °C and $T=125$ °C. $R_G^{EXT}=220 \Omega$ and $V_{DC}=600$ V, (b) Measured dI_{DS}/dt for the 42 A SiC MOSFET during turn-on as a function of the DC link voltage at 25 °C and 125 °C

The dI_{DS}/dt as a function of the DC link voltage, obtained from the turn-on transients shown in Figure 3.40, is shown in Figure 3.41(b). Analysing the switching rate values, it can be seen that the temperature sensitivity of the switching rate is constant for the different DC voltages evaluated.

The measured switching rates and increases with temperature for the evaluated DC link voltages are shown in Table 3-IV. As the DC voltage is increased from 75 V to 600 V, dI_{DS}/dt increases with temperature by 19 %. However, as the nominal switching

rate is affected by the DC link voltage value, the use of dI_{DS}/dt as TSEP would require an initial calibration.

Table 3-IV Switching rates at 25 °C and 125 °C for different DC link voltages

DC link voltage, V_{DC} (V)	dI_{DS}/dt , $T=25\text{ }^{\circ}\text{C}$ (A/ μs)	dI_{DS}/dt , $T=125\text{ }^{\circ}\text{C}$ (A/ μs)	Increase (%)
75	40.54	48.14	18.7
150	44.59	53.48	20.0
300	48.44	58.01	19.7
600	52.55	62.32	18.7

Other important factor is the evaluation of the impact of the load current on the temperature sensitivity of both the switching rate and the gate current plateau. Figure 3.42(a) presents the turn-on drain-source current characteristics of the 42 A SiC power MOSFET switched with $R_G^{EXT}=220\text{ }\Omega$ for 3 different load currents, namely 5, 13 and 21 A, at a temperature of 25 °C, while Figure 3.42(b) shows the corresponding gate current characteristics of the SiC MOSFET during turn-on. These characteristics were measured at a higher temperature, namely 125 °C, and the captured I_{DS} and I_G turn-on transients are shown in Figure 3.43(a) and Figure 3.43(b) respectively.

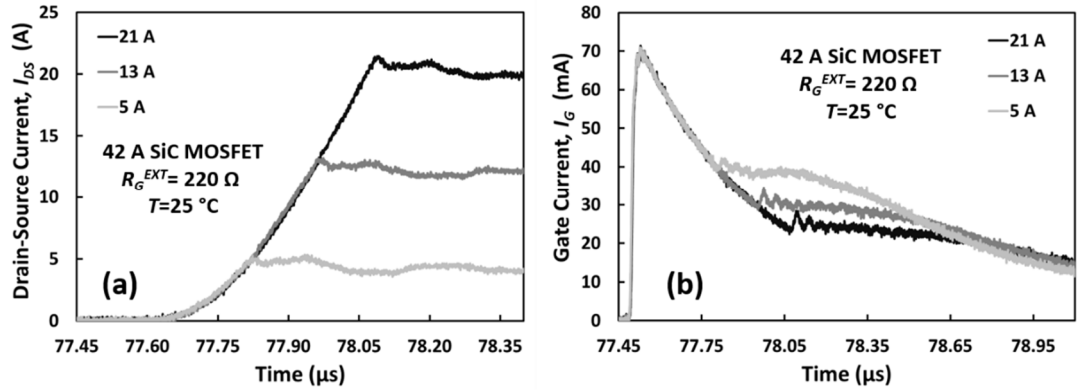


Figure 3.42 (a) Measured I_{DS} turn-on transients for different load current values for the 42 A SiC MOSFET at 25 °C, (b) Measured I_{GS} turn-on transients for different load currents for the 42 A SiC MOSFET at 25 °C

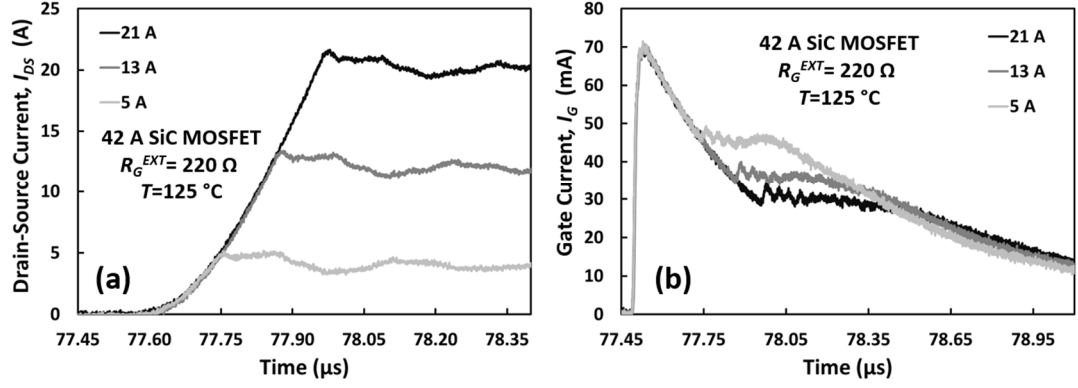


Figure 3.43 (a) Measured I_{DS} turn-on transients for different load current values for the 42 A SiC MOSFET at 125 °C, (b) Measured I_{GS} turn-on transients for different load currents for the 42 A SiC MOSFET at 125 °C

Analysing the drain-source current and gate current transients in Figure 3.42 and Figure 3.43, it is observed that the instantaneous switching rate of I_{DS} is independent of the load current. However, the gate current plateau is inversely proportional to the load current. Since the gate current plateau occurs at the time instant when I_{DS} reaches the load current, then for the same switching rate, the gate current plateau will increase with decreasing load current. This is due to the fact that the transition point of the gate current from the $C_{GS} + C_{GD-HV}$ (low Miller capacitance) charging phase to the $C_{GS} + C_{GD-LV}$ (high Miller capacitance) charging phase occurs after the full load current has been reached.

In the case of the gate current plateau, for a known load current, the junction temperature can be deduced from the plateau value, especially when a high R_G^{EXT} is used as shown by the results in Figure 3.42 and Figure 3.43. If the load current is changing, using the gate current plateau as a TSEP will require separating the effect of the junction temperature change from the effect of the load current variation. As it is shown in Figure 3.44 it is possible to measure the same gate current plateau at 2 different junction temperatures and load currents. As the results on Figure 3.44 show, a gate current plateau of 30 mA results from a load current of 21 A at 125 °C and from a load current of 13 A and a junction temperature of 25 °C.

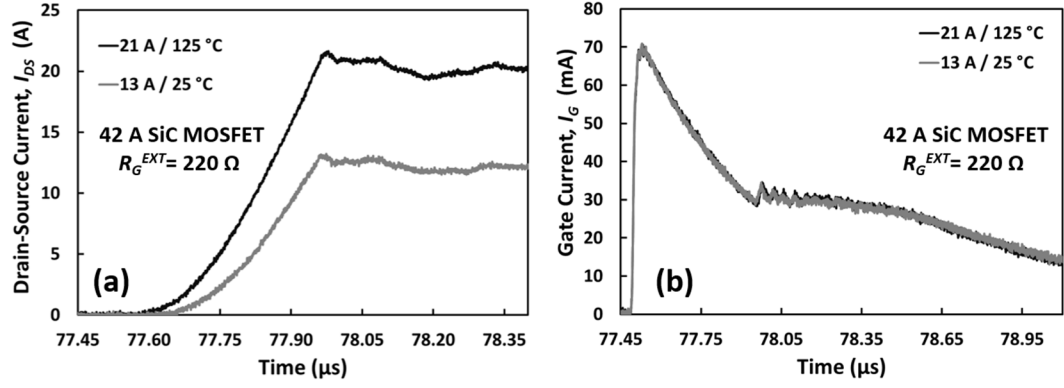


Figure 3.44 (a) Measured I_{DS} turn-on transients of the 42 A SiC MOSFET for a load current of 13 A at 25 °C and a load current of 21 A at 125 °C, (b) Measured I_G turn-on transients of the 42 A SiC MOSFET for a load current of 13 A at 25 °C and a load current of 21 A at 125 °C

The gate current plateau (I_{GP}) can be calculated from the gate current characteristics shown in Figure 3.17 at the time instant when the gate current transient changes from the gate-source capacitance charging component to the Miller capacitance charging component and it can be expressed as

$$I_{GP} = \frac{C_{GS}}{(C_{GS} + C_{GD-HV})} \cdot \frac{V_{GG}}{(R_G^{INT} + R_G^{EXT})} \cdot e^{-\frac{t_1 - t_0}{(R_G^{INT} + R_G^{EXT})(C_{GS} + C_{GD-HV})}} \quad (3.17)$$

where t_1 is the time when V_{GS} becomes equal to V_{GP} .

The time $t_1 - t_0$ can be expressed as the sum of the time it takes for V_{GS} to reach V_{TH} and the current rise time using equation (3.18).

$$t_1 - t_0 = t_{rise} + (t_{TH} - t_0) = \frac{I}{\left(\frac{dI_{DS}}{dt}\right)} + (t_{TH} - t_0) \quad (3.18)$$

where the current rise time is given by the ratio of the current to the switching rate and $t_{TH} - t_0$ is given by equation (3.3). According to equation (3.17) and equation (3.18) I_{GP} will increase with decreasing load current and increase with increasing junction temperature.

The use of the switching rate as TSEP has been presented in this chapter, however, using the switching rate as a TSEP requires the ability to measure high dI_{DS}/dt values. Recent power modules include current sensors embedded, hence, the evaluation of these

sensors for measuring temperatures in SiC power MOSFETs could be the next step. Intelligent gate drivers with closed loop control and dI/dt feedback and control have been presented and evaluated for IGBTs. In this intelligent gate drivers, the voltage across the parasitic inductance of the power module is used for measuring the switching rate [11, 28] thus requiring an auxiliary emitter connection. Recent advances in current sensors like Rogowski coils with high dI/dt detection [29] or magnetoresistive current sensors [30] suggest that the identification of the temperature by means of the switching rate can be feasible.

In the case of the magnetoresistive current sensors from Sensitec [31], they have a bandwidth of 3 MHz and, according to the information from the manufacturer, the models rated at 25 A and 50 A have a rise time of 50 ns for the nominal current, which is suitable for measuring the switching rates of the current transients evaluated here. The Rogowski coils presented in [29] are able to detect switching rates up to 5 kA/ μ s. Commercial current probes from PEM UK [32] based on Rogowski coils have a bandwidth of 30 MHz. The current probe Ultra Mini from PEM UK rated at 60 A has a measurable peak dI/dt of 4 kA/ μ s.

In the tests performed in this thesis the current sensor used was a Tektronix current probe model TCP-312, which is a split core current probe. Other suitable current sensors for the use in the laboratory are Pearson current probes and coaxial shunts [33, 34]. Both sensors have a high bandwidth, small rise time and would be suitable for using in the laboratory. The Pearson current probes [35] provide galvanic isolation however they saturate for large currents and they are not suitable for continuous DC operation. Coaxial shunts, for example the SDN-015 from T & M Research products [36] which has a bandwidth of 1200 MHz and a rise time of 0.3 ns, do not provide galvanic isolation.

The ability to change the gate drive resistance during operation [37], by using an intelligent programmable gate driver [38-40], could also enable this technique of junction temperature sensing without suffering the penalty of increased switching losses. The devices will be driven at high switching rates (using low gate drive resistances) and at the occasional instants when junction temperature sensing is required, a higher gate resistance is used for monitoring the temperature dependent switching parameters. Hence, the device switching rate will only be slowed down occasionally, when the junction

temperature measurement is performed. This approach has been successful using the turn-off delay as TSEP for SiC MOSFETs in [41].

In the case of slowing down the transient for the measurement sequence, an important point to take into consideration is that slowing down the switching transients for improving the sensitivity of a TSEP can have an impact in the operation of a converter, if the temperature is to be estimated online. Slowing down the turn-off transient can improve the temperature sensitivity of the turn-off delay of IGBTs and MOSFETs, as it was shown in section 3.1 but it could affect the operation of the converter in the case that fixed dead times are implemented. In the case of slowing down the turn-on for enabling the junction temperature measurement, if the turn-off of the transistor is done at the nominal switching rate, the use of fixed dead times would not be affected.

Another important point about the use of this dI_{DS}/dt for online condition monitoring of a converter is the noisy environment, which can affect the measurement of fast transient signals causing spurious measurements and making the implementation of this TSEP for on-line condition monitoring challenging. However, the results presented in this thesis suggest that it could be a suitable TSEP for off-line condition monitoring

Considering a power module, where usually multiple chips are paralleled for increasing the current capability, the question of how the temperature imbalance can affect the temperature estimation using TSEPs arises. Chapter 4 will evaluate the impact of having multiple chips in parallel on the use of TSEP for the estimation of the junction temperature. Moreover, the estimation of the junction temperature by means of TSEPs requires a good sensitivity. Some electrical parameters, like the on-state resistance of a MOSFET, are affected by the gate driver voltage. The studies presented in chapter 4 present how the temperature sensitivity can be improved by means of the gate driver voltage, highlighting the importance of intelligent gate drivers for health monitoring.

3.7 Summary

The temperature sensitivity of SiC power devices has been evaluated in this chapter, with the turn-on current switching rate (dI_{DS}/dt) and the gate current transient presented as TSEPs which could be used for enabling on-line condition monitoring.

In the case of silicon MOSFETs, the negative temperature coefficient of threshold voltage is balanced by the negative temperature coefficient of the channel mobility, hence, dI_{DS}/dt is temperature invariant. However, in the case of SiC power MOSFETs both the turn-on dI_{DS}/dt and the gate current plateau increase linearly with temperature. The negative temperature coefficient of the threshold voltage together with the temperature invariance of the channel mobility in the evaluated temperature range are the reason behind the positive temperature coefficient of dI_{DS}/dt , as the analytical models presented in this chapter show. It has also been presented how the parasitic source inductance hinders the temperature sensitivity of dI_{DS}/dt and I_{GP} when the devices are switched at high speed.

The impact of the DC link voltage and the load current, which are defined by the application, on the temperature sensitivity of the proposed TSEPs has also been evaluated in this chapter. The switching rate increases with the DC link supply voltage, meaning that the use of the switching rate as TSEP will require an initial calibration. However, for DC link voltages ranging from 75 to 600 V it has been shown that the temperature sensitivity is similar, resulting in an increase of the switching rate of around 20 % when the temperature increases from 25 °C to 125 °C. In the case of the gate current plateau and its transients, there is a dependency on both the temperature and the load current. Decoupling of the effect of the load current and temperature would be necessary in order to implement effective junction temperature identification.

To exploit the benefits of SiC power devices fast switching is recommended, however, reducing the switching rate improves the temperature sensitivity of the proposed TSEPs. Two suitable options for tackling this barrier have been identified: sacrificing the switching speed of the device at the expense of higher switching losses or the use intelligent gate drivers with the capability of variable gate drive impedance. In this case the devices would be slowed down occasionally to perform the junction temperature sensing when the information is required.

3.8 References

- [1] J. Millán, P. Godignon, Xavier Perpiñà, Amador Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, 2014.
- [2] H. Luo, W. Li, and X. He, "Online high-power P-i-N diode chip temperature extraction and prediction method with maximum recovery current di/dt ," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2395-2404, 2015.
- [3] H. Luo, Y. Chen, W. Li, and X. He, "Online High-Power p-i-n Diode Junction Temperature Extraction With Reverse Recovery Fall Storage Charge," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2558-2567, 2017.
- [4] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1478-1483.
- [5] A. Koenig, T. Plum, P. Fidler, and R. W. D. Doncker, "On-line Junction Temperature Measurement of CoolMOS Devices," in *2007 7th International Conference on Power Electronics and Drive Systems*, 2007, pp. 90-95.
- [6] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5122-5132, 2016.
- [7] S. Jahdi, O. Alatise, P. Alexakis, L. Ran, and P. Mawby, "The impact of temperature and switching rate on the dynamic characteristics of silicon carbide Schottky barrier diodes and MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 163-171, 2015.
- [8] C. DiMarino, "High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power Semiconductor Transistors," Master of Science in Electrical Engineering, Virginia Polytechnic Institute and State University, 2014.
- [9] D. Barlini, M. Ciappa, A. Castellazzi, M. Mermet-Guyennet, and W. Fichtner, "New technique for the measurement of the static and of the transient junction temperature in IGBT devices under operating conditions," *Microelectronics Reliability*, vol. 46, no. 9, pp. 1772-1777, 2006/09/01 2006.
- [10] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors* 2nd ed.: SEMIKRON International GmbH, 2015.
- [11] Y. Lobsiger and J. W. Kolar, "Closed-Loop di/dt and dv/dt IGBT Gate Driver," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3402-3417, 2015.
- [12] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2008.
- [13] A. D. Pathak, *MOSFET/IGBT drivers theory and applications*. Available: <http://www.ixys.com/documents/appnotes/ixan0010.pdf> (Access: 1/05/2017).
- [14] C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, and P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," in *IEEE Energy Conversion Congress and Exposition ECCE*, 2013, pp. 3235-3242.

- [15] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1986-1997, 2014.
- [16] Infineon. *AN2003-3 Switching behaviour and optimal driving of IGBT³ modules*. Available: <http://www.infineon.com/dgdl/Infineon+-+AN2003-03+-+Switching+behaviour+and+optimal+driving+of+IGBT3+modules.pdf?fileId=d3a304412b407950112b40ee84712c4> (Access: 7/07/2017).
- [17] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IGBT junction temperature measurement via peak gate current," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3784-3793, 2016.
- [18] H. Niu and R. D. Lorenz, "Sensing power MOSFET junction temperature using gate drive turn-on current transient properties," *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1677-1687, 2016.
- [19] M. Denk and M. M. Bakran, "An IGBT Driver Concept with Integrated Real-Time Junction Temperature Measurement," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1-8.
- [20] M. Denk and M. M. Bakran, "Junction Temperature Measurement during Inverter Operation using a TJ-IGBT-Driver," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1-8.
- [21] Z. Chen, Y. Yao, M. Danilovic, and D. Boroyevich, "Performance evaluation of SiC power MOSFETs for high-temperature applications," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012.
- [22] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876-884, 2001.
- [23] M. Hasanuzzaman, S. K. Islam, L. M. Tolbert, and M. T. Alam, "Temperature dependency of MOSFET device characteristics in 4H- and 6H-silicon carbide (SiC)," *Solid-State Electronics*, vol. 48, no. 10–11, pp. 1877-1881, October 2004.
- [24] J. A. B. Ccoa, B. Strauss, G. Mitic, and A. Lindemann, "Investigation of Temperature Sensitive Electrical Parameters for Power Semiconductors (IGBT) in Real-Time Applications," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1-9.
- [25] J. Wang, H. S. h. Chung, and R. T. h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573-590, 2013.
- [26] A. Elbanhawy. *Effect of source inductance on MOSFET rise and fall times*. Available: <http://www.maplesoft.com/applications/view.aspx?SID=5730> (Access: 16/07/2017).

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- [27] B. J. Baliga, "Chapter 9 - IGBT Applications: Transportation," in *The IGBT Device*, ed Amsterdam: William Andrew Publishing, 2015, pp. 223-275.
 - [28] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3720-3732, 2014.
 - [29] A. Ahmed, L. Coulbeck, A. Castellazzi, and C. M. Johnson, "Design and test of a PCB Rogowski coil for very high dI/dt detection," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012.
 - [30] R. Slatter, M. Brusius, and H. Knoll, "Magnetoresistive current sensors as an enabling technology for ultra-high power density electric drives," presented at the 9th International Conference on Integrated Power Electronics Systems, 2016.
 - [31] Sensitec. *CMS3000 family AMR current sensors with 2 MHz bandwidth*. Available: <https://www.sensitec.com/products-solutions/current-measurement/cms3000-family> (Access: 21/10/2017).
 - [32] PEM UK. Available: <http://www.pemuk.com/> (Access: 21/10/2017).
 - [33] Fred Wang, Zheyu Zhang, and Edward A. Jones, "Wide Bandgap Device Characterization," presented at the APEC, 2016.
 - [34] Z. Zhang, "Characterization and Realization of High Switching-speed Capability of SiC Power Devices in Voltage Source Converter," PhD dissertation, University of Tennessee, 2015.
 - [35] Pearson and Electronics. *Wideband Current Monitors*. Available: <http://www.pearsonelectronics.com/products/wideband-current-monitors> (Access: 22/10/2017).
 - [36] T & M Research Products. Available: <http://www.tandmresearch.com/> (Access: 22/10/2017).
 - [37] Andreas Volke and M. Hornkamp, *IGBT modules. Technologies, driver and application*, Second ed.: Infineon Technologies AG, 2012.
 - [38] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, *et al.*, "General-purpose clocked gate driver (CGD) IC with programmable 63-level drivability to reduce I_c overshoot and switching loss of various power transistors," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1640-1645.
 - [39] A. Shorten, W. T. Ng, M. Sasaki, T. Kawashima, and H. Nishio, "A segmented gate driver IC for the reduction of IGBT collector current over-shoot at turn-on," in *2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2013, pp. 73-76.
 - [40] B. Ji, W. Cao, and V. Pickert, "State-of-the-art intelligent gate drivers for IGBT power modules - monitoring, control and management at the heart of power converters," in *Control Circuits in Power Electronics: Practical issues in design and implementation*, ed: Institution of Engineering and Technology, 2016, pp. 307-335.

- [41] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, B. J. Blalock, and X. Wu, "Online junction temperature monitoring using turn-off delay time for silicon carbide power devices," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7.

4 Additional considerations on the use of TSEPs for junction temperature identification

4.1 Introduction

In previous chapters of this thesis, both classic and more novel TSEPs have been presented and evaluated. In chapter 3, the switching rate of the turn-on current was identified as a potential TSEP for condition monitoring in SiC power MOSFETs. The forward voltage of SiC Schottky diodes was also evaluated as a TSEP, which is a well established TSEP, widely used in power cycling test, as it was used in chapter 2.

The measurements and results presented were for discrete power devices. However, in applications where condition monitoring will be useful, the power devices will typically be in the form of parallel connected devices, in a multi-chip power module. For SiC power devices where the maximum current ratings are low, the need to parallel devices is more pressing for high current applications.

Figure 4.1 (a) shows the internal view of a 1200V/150A silicon IGBT/PiN diode half-bridge power module from Dawin Electronics, with datasheet number DM2G100SH12AE where, as can be seen, the high side and low side devices are comprised of single chips. Figure 4.1(b) shows the internal view of a similarly rated 1200V/168A SiC half-bridge power module from CREE/Wolfspeed, with datasheet number CAS100H12AM1 where five parallel MOSFETs and five parallel diodes are required for conducting the 168 A full current [1]. The reason why paralleling is much more prevalent in SiC devices compared with silicon is the fact that the maximum current rating of single SiC devices is much smaller than silicon. This is because of limited device yield in SiC fabrication processes, difficulties in defect density control and the expensive nature of the SiC wafer [2]. Nevertheless, this is not exclusive to SiC devices. There are many IGBT modules with parallel chips for enabling very high current capability like the 1700 V/1000 A half-bridge module FF1000R17IE4 from Infineon [3]. The structure of a power module with multiple Si IGBTs and diodes in parallel is shown in Figure 4.2 [4].

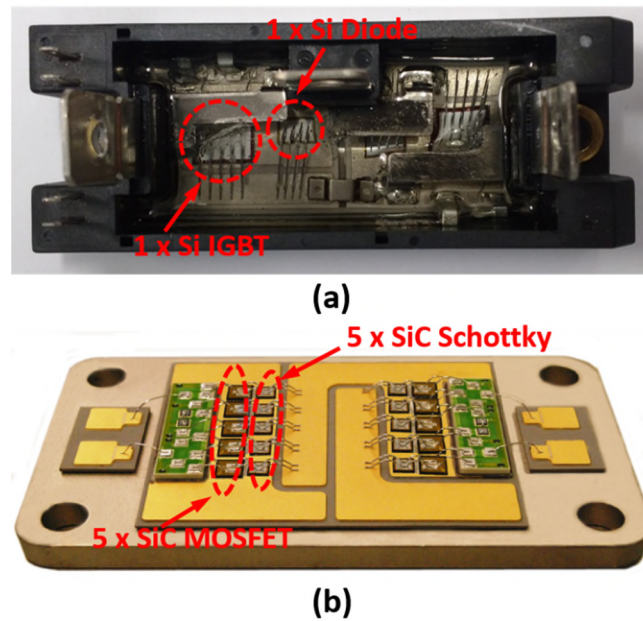


Figure 4.1 (a) Internal view of a Si IGBT half-bridge module (b) Internal view of a SiC MOSFET half-bridge module [1]

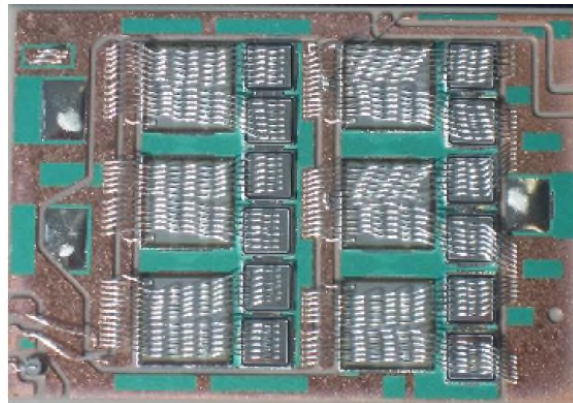


Figure 4.2 Internal view of a Si IGBT/diode power module with multiple chips in parallel [4]

Given the emergence of SiC MOSFET modules and high current IGBT modules, which require multiple chips in parallel as mentioned before, the use of temperature sensitive parameters for multiple chips in parallel is a recent topic of interest which has been studied by different researchers, for example [5, 6] where Si IGBTs have been studied.

The use of the temperature sensitive electrical parameters at module level where multiple chips are paralleled should be assessed. These chips could have different electrothermal characteristics and, in addition, there can be differential degradation

among them. Hence, it is necessary to investigate the impact of die-to-die variation in parallel connected devices on junction temperature estimation using TSEPs and its impact on the effectiveness of the TSEP. In this chapter, the impact of electrothermal variation between parallel connected devices on the effectiveness of the TSEP is investigated for both silicon bipolar and SiC unipolar technologies.

Moreover, the sensitivity of a TSEP would be key for enabling effective junction temperature estimation. The on-state resistance of a SiC MOSFET is strongly dependent on the gate-source voltage, requiring a higher voltage compared with Si devices for achieving at low on-state resistance value. The impact of the gate driver voltage on the temperature sensitivity of SiC MOSFETs is investigated in this chapter, in an effort to maximise the temperature sensitivity of both the on-state resistance and the current switching rate as TSEPs.

4.2 Impact of parallel devices on the TSEP effectiveness

4.2.1 *Forward voltage as TSEP for parallel diodes*

Referring back to chapter 2, the on-state voltage at low currents is a well-known and established TSEP for both silicon and silicon carbide devices. At low currents, the forward voltage across a diode, the collector-emitter voltage across an IGBT and the forward voltage across the body diode of a MOSFET have a negative temperature coefficient temperature as a result of thermally induced carriers from bandgap narrowing [7].

This TSEP has been widely used for identifying the junction temperature during power cycling tests [8]. Some examples of its use are [9], where the estimated junction temperature is used for monitoring the thermal impedance degradation and the T3ster [10], dedicated power cycling and thermal impedance characterisation equipment, where it is one of the TSEPs used for monitoring the junction temperature during power cycling studies. However, the use of this TSEP requires an initial calibration. The forward voltage across the device is measured at different temperatures, using a low value sensing current which should have negligible self-heating effects. For this calibration procedure, the

temperature of the device is set externally, allowing enough time to reach a steady state, hence the junction temperature can be considered equal to this temperature.

Using the experimental setup for calibration of the forward voltage as TSEP presented in chapter 2, the calibration curves for a Si PiN diode and SiC Schottky diode were obtained for a sensing current I_{SENSE} of 50 mA. The selected devices are a 600 V Si PiN diode from International Rectifier, with a current rating of 4 A at 100 °C and datasheet reference HFA04TB60, and a 600 V SiC Schottky diode from Cree/Wolfspeed, with a current rating of 4 A at 135 °C and datasheet reference C3D02060A. Both devices are discrete TO-220 package devices and the calibration results are presented in Figure 4.3.

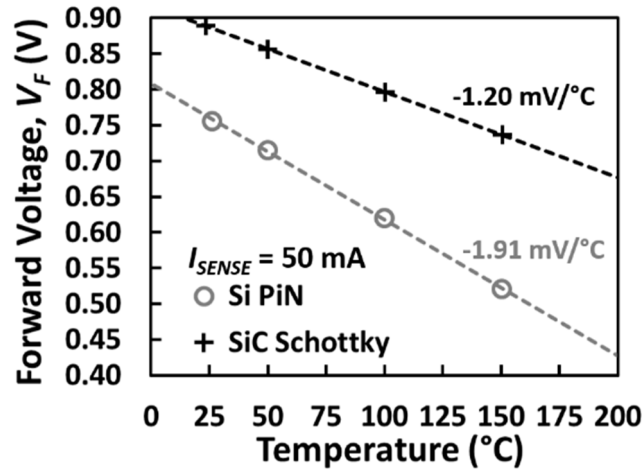


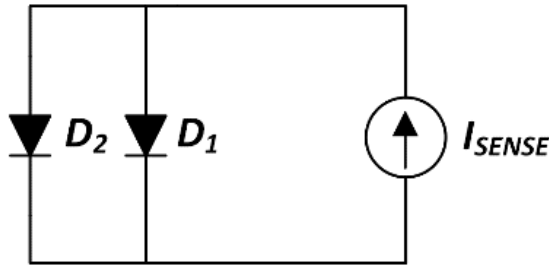
Figure 4.3 Calibration curves for on-state voltage as TSEP. Single Si PiN and SiC Schottky diodes.
 $I_{SENSE}=50$ mA

One of the main benefits of this TSEP is that it allows to capture the cooling or heating transient, enabling the evaluation of the thermal impedance and its degradation during power cycling tests [9, 11, 12]. The limited current conduction capability of SiC, determined by the reduced chip size, requires parallel connection of multiple chips for increasing the current rating. This can be done paralleling devices in discrete packages, as well as in higher current modules, where multiple dies are used in parallel.

In this situation, a difficulty arises in the interpretation of the on-state voltage as TSEP since a single forward voltage is measured. If the parallel devices have different junction temperatures due to a variation in the thermal resistances caused by different degradation of the packaging, the reading of a single temperature may not give an accurate

interpretation of the junction temperature, hence the impact of the temperature imbalance on the estimated junction temperature should be studied.

For the studies performed in this chapter, discrete devices connected in parallel were used, allowing the control of the temperature of each chip independently and limiting the thermal coupling between the chips since they do not share the same substrate or heater. A modified version of the calibration circuit presented in chapter 2 was used for this new calibration, with the schematic shown in Figure 4.4(a). The calibration of the forward voltage has been done setting the temperature of each device at the same value using the individual DC heaters described in chapter 2, as shown in Figure 4.4(b). The sensing current used for this calibration was $I_{SENSE} = 50$ mA and the calibration curve for parallel diodes is presented in Figure 4.5. The sensing current was measured using a digital multimeter Fluke 175, the forward voltage was measured using a digital multimeter HAMEG model HMC8012 and the temperature was captured using a thermocouple data logger model TC-08 from Pico Technology.



(a)



(b)

Figure 4.4 (a) Electrical schematic for calibration of the on-state voltage as TSEP for parallel diodes, (b) Detail of the heaters for controlling the individual temperature

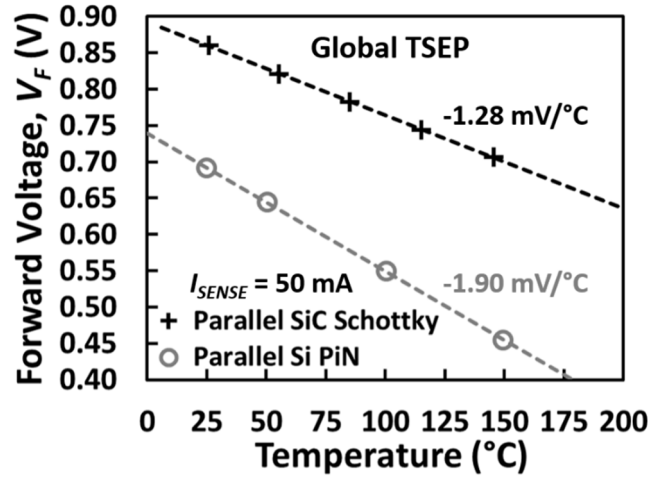


Figure 4.5 Calibration curves for on-state voltage as TSEP. Parallel Si PiN and SiC Schottky diodes.
 $I_{SENSE}=50$ mA

The calibration curve shown in Figure 4.5 was measured for a sensing current of 50 mA. Assuming equal temperature and identical diodes, the sensing current should be shared equally by both diodes, hence the current flowing through each diode should be 25 mA. The measured calibration curve for a single diode and a sensing current I_{SENSE} of 25 mA is shown in Figure 4.6.

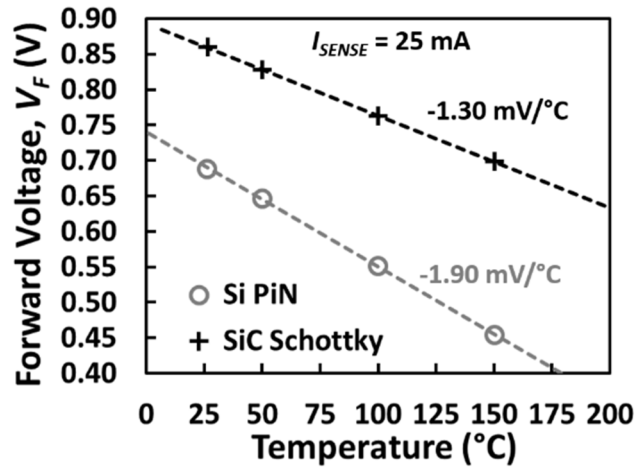


Figure 4.6 Calibration curves for on-state voltage as TSEP. Single Si PiN and SiC Schottky diode.
 $I_{SENSE}=25$ mA

Comparing Figure 4.5 and Figure 4.6, it can be observed that the slope of the calibration curve (-1.90 mV/°C) is identical for the parallel PiN diodes using a sensing current of 50 mA and the single diode using a sensing current of 25 mA. In the case of the SiC Schottky diodes, there is a slight difference between the calibration curves of the

single diode ($-1.30 \text{ mV}/^\circ\text{C}$) and the parallel diodes ($-1.28 \text{ mV}/^\circ\text{C}$). This difference can be attributed small differences between the parallel diodes or the circuit.

In [13] it is stated that the use of the on-state voltage as TSEP gives an average temperature of the chips, but it is important to evaluate the accuracy of this average temperature estimation. Using the test configuration shown in Figure 4.4, thermal imbalance was introduced between the parallel diodes by setting different case temperatures by means of the external heaters.

In the first test, the temperature of D_1 was fixed at the ambient temperature of 25°C , while the temperature of D_2 was increased up to 145°C using the heater. This test was performed for both Si and SiC diodes and the case temperatures, as well as the forward voltage across the paralleled diodes were logged during heating transient. The measured transient characteristics for the parallel SiC Schottky and Si PiN diodes are shown in Figure 4.7 and Figure 4.8 respectively.

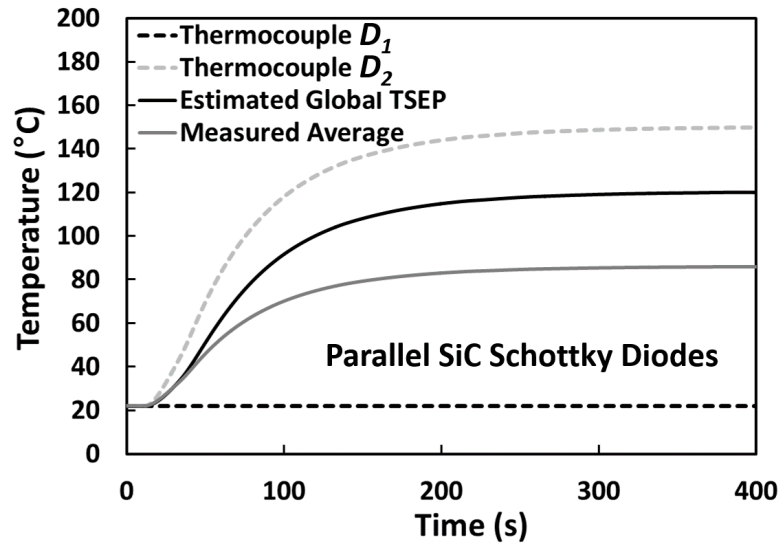


Figure 4.7 Transient heating of parallel SiC Schottky diodes. Measured case temperatures and estimated junction temperature

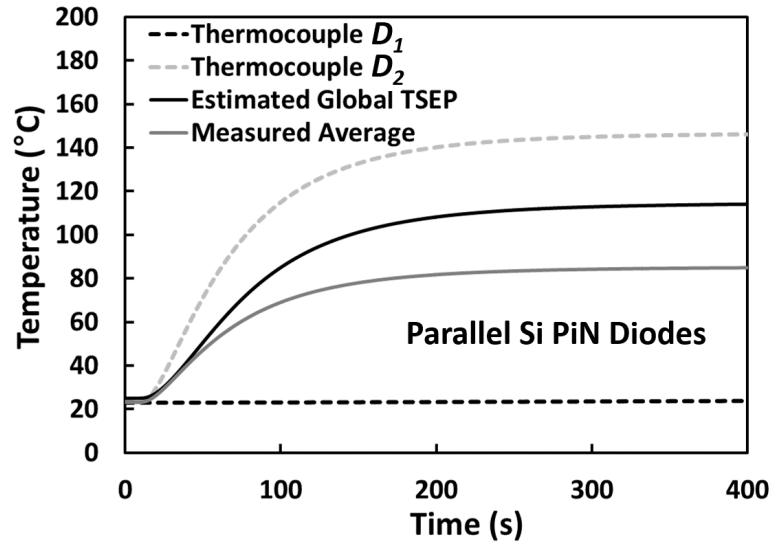


Figure 4.8 Transient heating of parallel Si PiN diodes. Measured case temperatures and estimated junction temperature

Figure 4.7 and Figure 4.8 show the measured temperature values for the parallel diodes, their numerical average and the estimated temperature using the TSEP for the parallel diodes, otherwise known as the global TSEP (as shown in Figure 4.5). From these transient measurements, it can be seen that the measured numerical average is close to the global TSEP estimation during the initial stages of the transient. However, as the temperature difference increases, the temperature estimated using the global TSEP is higher than the numerical measured average but it under-estimates the temperature of the hotter device.

The plots presented in Figure 4.7 and Figure 4.8 show the transient heating of one diode. In order to eliminate the transient effects and ensure that the temperature of the semiconductor chip can be assumed equal to the temperature of the case (controlled by the external heater) investigations at steady state for different temperature imbalances have been performed.

The value of the sensing current is below the Zero Temperature Coefficient (ZTC) [7, 13], meaning that the hotter device will conduct more current, however, the calibration of the on-state voltage assumes that the sensing current is shared equally by both devices. The current distribution between diodes, at steady state for different temperature imbalances, has been measured and it is shown in Figure 4.9 and Figure 4.10. Figure 4.9 shows the current distribution between two parallel SiC Schottky diodes while Figure

4.10 presents the current distribution for two parallel Si PiN diodes. The total sensing current of 50 mA was measured using a digital multimeter Fluke 175 and the current through the hotter device was measured using current probe Tektronix model TCP-303.

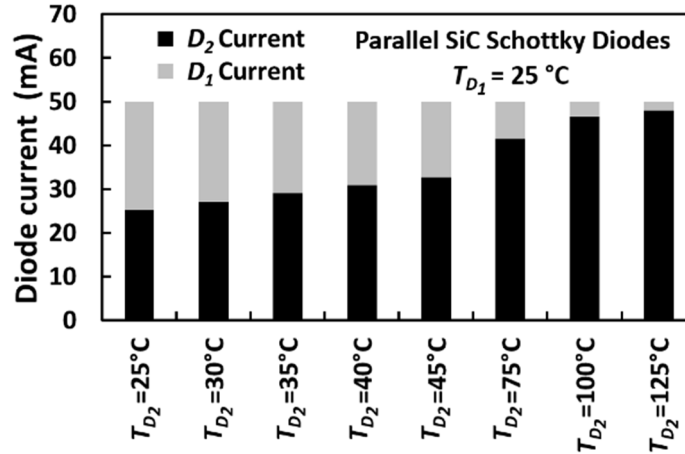


Figure 4.9 Sensing current distribution for temperature imbalance between parallel SiC Schottky diodes

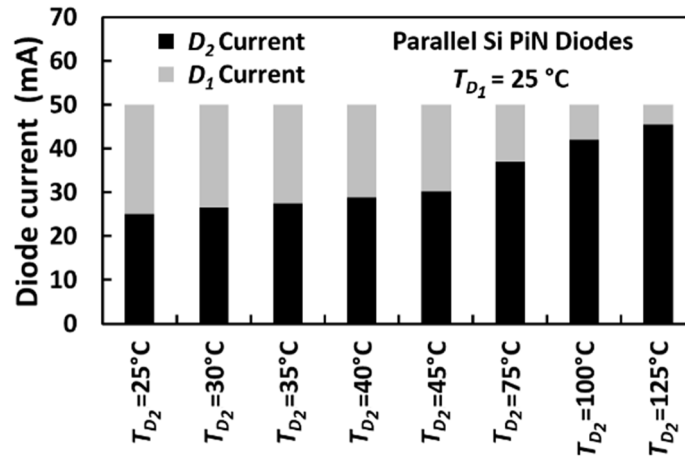


Figure 4.10 Sensing current distribution for temperature imbalance between parallel Si PiN diodes

As it is clearly observed from the results presented in both Figure 4.9 and Figure 4.10, the impact of having a sensing current below the ZTC causes the current to flow mainly through the hotter device as the temperature difference between the diodes increases. This effect is more apparent on the evaluated SiC Schottky. This current imbalance caused by the difference in temperature between the parallel chips can cause errors in the temperature estimation using the on-state voltage as a TSEP when multiple dies are paralleled, as the measurement scenario is different to the calibration one.

It is important to remark that the minimum measurable current, according to the current probe datasheet is 5 mA, hence there could be some precision issues with the exact value of the sensing current, as the current measured ranges from 25 mA to 50 mA. The measurements were performed different times and the trend of the current flowing mainly through the hotter diode for the high temperature imbalance was confirmed.

Measurements have been performed to evaluate the impact of the temperature imbalance on the junction temperature estimation using the forward voltage as TSEP. Using the experimental setup shown in Figure 4.4, the temperature of diode D_1 (T_{D1}) was fixed at 86 °C using one of the available heaters, while the temperature of diode D_2 (T_{D2}) was adjusted to a higher temperature, hence setting a defined and controlled junction temperature imbalance. The temperatures selected for T_{D2} were 91, 96, 101, 106 and 150 °C. This experiment was performed for both the parallel Si PiN diodes and the SiC Schottky diodes, recording the forward voltage for a sensing current $I_{SENSE}=50$ mA and the case temperatures. The measurements were performed at steady state, hence the case temperature and the junction temperature can be considered equal.

Using the measured forward voltage, the junction temperature can be estimated using the global TSEP, given by the calibration curves shown in Figure 4.5, which assumes equal sensing current distribution between the diodes. This estimated junction temperature value is compared with the numerical average temperature of the diodes (which is set by the heaters) for both SiC and Si devices in Figure 4.11 and Figure 4.12 respectively.

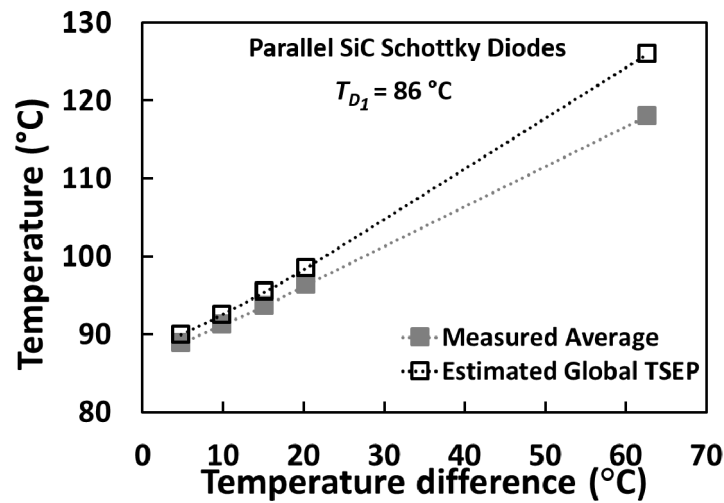


Figure 4.11 Measured averaged temperature and estimated average temperature for parallel SiC Schottky diodes

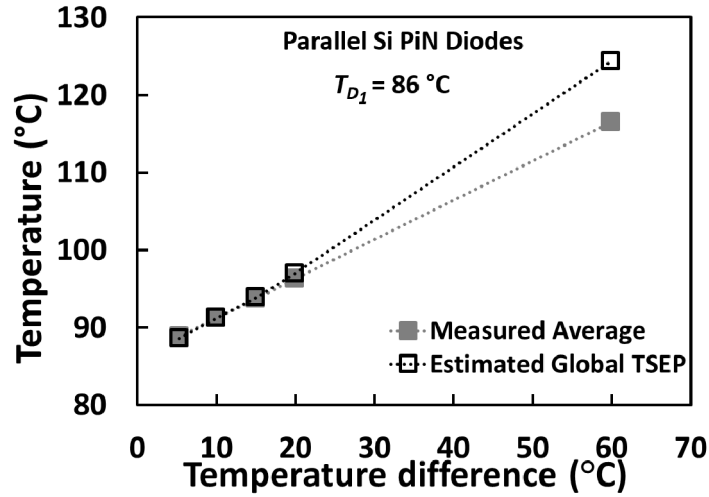


Figure 4.12 Measured averaged temperature and estimated average temperature for parallel Si PiN diodes

As the results presented in Figure 4.11 and Figure 4.12 show, for a small temperature difference between the parallel diodes, the temperature estimated by the global TSEP gives an accurate estimation of the average temperature. However, as the temperature difference increases, the accuracy of the global TSEP reduces. Considering that the health condition of the module will be determined by the chip with a higher thermal resistance, this has important implications on the health characterisation of the power module. Hence, the use of this global TSEP will be limited for identifying the most degraded chip in a module with multiple parallel chips.

Referring back to Figure 4.9 and Figure 4.10, an important factor that can be identified is that as the temperature difference increases, the sensing current flows mainly through the hotter diode, i.e. the sensing current of 50 mA circulates mainly through a single diode. Using the TSEP calibrated using a single diode and a sensing current of 50 mA, as defined by the calibration curves in Figure 4.3, the junction temperature of the imbalanced parallel diodes can be estimated. Since this TSEP corresponds to a single diode rather than a connection of parallel diodes, this can be considered to be a local TSEP. The temperature of each of the parallel diodes and the estimated junction temperatures using the aforementioned local and global TSEPs are shown Figure 4.13 in for the parallel SiC Schottky diodes, while Figure 4.14 show the same characteristics for the parallel Si PiN diodes.

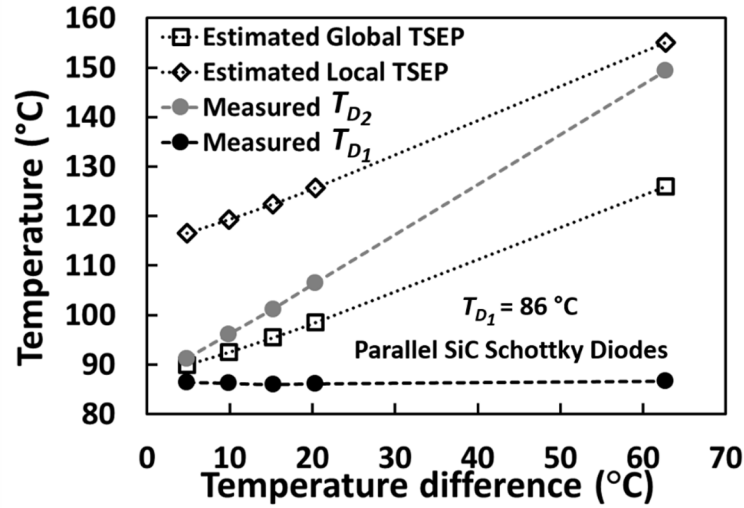


Figure 4.13 Measured temperatures of the parallel SiC Schottky diodes and estimated temperatures using the local and global TSEPs

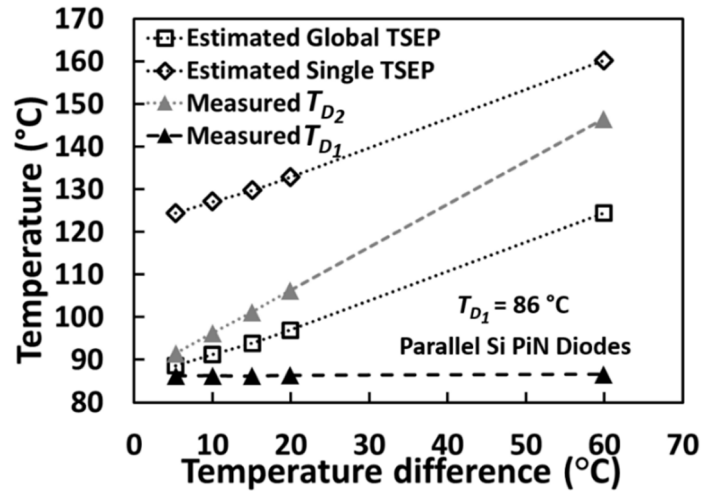


Figure 4.14 Measured temperatures of the parallel Si PiN diodes and estimated temperatures using the local and global TSEPs

From the results presented in Figure 4.13 and Figure 4.14, an interesting observation is that the local TSEP is more accurate in predicting the temperature of the hottest diode for high temperature differences between the parallel chips, given that the sensing current flows mainly through the hotter diode. However, for low temperature differences between the parallel devices, the global TSEP is more accurate in predicting the temperature of the hotter device. Hence, the global TSEP always under-estimates the temperature of the hotter device while the local TSEP over-estimates. This is clearly observed for both technologies, in Figure 4.13 and Figure 4.14. The results presented in

these two figures are summarised in Table 4-I and Table 4-II, where the sensing current through the hotter device is also presented.

Table 4-I Effect of temperature imbalance between parallel SiC Schottky diodes on the junction temperature estimation using the on-state voltage at low current as TSEP

T_{D1} (°C)	T_{D2} (°C)	Average Measured Temperature (°C)	Forward Voltage $I_{SENSE}=50\text{mA}$ (V)	Global TSEP Estimation (°C)	Local TSEP Estimation (°C)	Sensing current – Hot device (mA)
86.4	91.2	88.8	0.7768	89.9	116.5	26.7
86.2	96.1	91.2	0.7735	92.5	119.3	28.9
86.0	101.2	93.6	0.7697	95.5	122.4	30.4
86.2	106.5	96.3	0.7658	98.5	125.7	32.2
86.7	149.4	118.0	0.7305	126.0	155.0	43.1

Table 4-II Effect of temperature imbalance between parallel Si PiN diodes on the junction temperature estimation using the on-state voltage at low current as TSEP

T_{D1} (°C)	T_{D2} (°C)	Average Measured Temperature (°C)	Forward Voltage $I_{SENSE}=50\text{mA}$ (V)	Global TSEP Estimation (°C)	Local TSEP Estimation (°C)	Sensing current – Hot device (mA)
86.2	91.5	88.9	0.5711	88.6	124.5	26.3
86.3	96.3	91.3	0.5661	91.2	127.1	27.7
86.2	101.2	93.7	0.5610	93.9	129.8	29.6
86.3	106.3	96.3	0.5551	97.0	132.9	30.7
86.6	146.5	116.6	0.5030	124.4	160.2	39.5

Referring back to Figure 4.7 and Figure 4.8, the final steady state of the heating transient can be considered a case of extreme temperature imbalance, where the temperature of one of the diodes was kept at ambient while the second diode was heated up to a temperature of around 150 °C. As the temperature estimation presented in Table 4-III shows, the local TSEP gives an accurate temperature estimation of the temperature of the hottest chip, while the accuracy of the global TSEP for estimating the average temperature is limited.

Table 4-III: Temperature estimation using the global and local TSEP in case of extreme imbalance

for parallel Si PiN and parallel SiC Schottky diodes

	T_{D1} (°C)	T_{D2} (°C)	Average Temperature (°C)	Forward Voltage $I_{SENSE}=50\text{mA}$ (V)	Global TSEP Estimation (°C)	Local TSEP Estimation (°C)
Parallel Si PiN diodes	23.8	146.3	85.0	0.5222	114.3	150.1
Parallel SiC Schottky diodes	22.1	150.0	86.0	0.7378	120.3	149.0

4.2.2 Reverse recovery as a TSEP for parallel diodes:

In the previous section of this chapter the impact of temperature imbalance between parallel chips for a well-known static TSEP like the forward voltage of a diode at low current was analysed.

The reverse recovery of Si PiN diodes is a dynamic TSEP, which was described in chapter 2. Some authors are using this TSEP for estimating the junction temperature [14, 15], however it is important to evaluate how the temperature difference between parallel diodes will affect the effectivity of this TSEP for junction temperature estimation.

The reverse recovery of parallel connected silicon PiN diodes and SiC Schottky diodes can be studied as a function of the temperature using the double pulse test configuration shown in Figure 4.15, which is a modification of the test setup presented in chapter 2. The ability of setting the temperature of each chip individually using the available DC heaters allows the study of the impact of junction temperature imbalance on the turn-off transient.

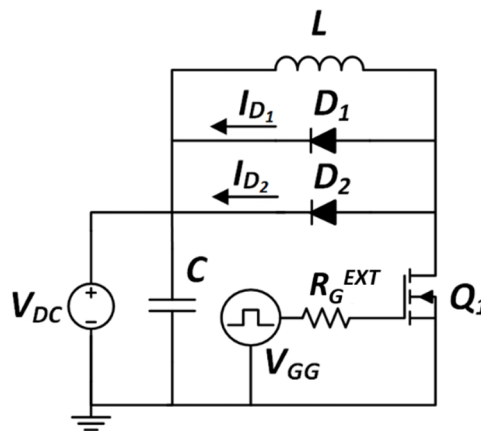


Figure 4.15 Double pulse test setup for evaluation of the reverse recovery of the clamping diodes

The devices selected for this study are 600 V silicon PiN diodes from International Rectifier with a current rating of 15 A at 140 °C, with datasheet reference 15ETH06 and 600 V SiC Schottky diodes from Cree/Wolfspeed, datasheet reference C3D06060A and a current rating of 9 A at 135 °C.

For the experiments presented in this section, the test values selected are DC link voltage $V_{DC} = 200$ V, inductor $L = 2$ mH, DC link capacitor $C = 470$ μ F, gate driver voltage $V_{GG} = 18$ V. The driving device Q_I is a Cree/Wolfspeed 1200V/42 A SiC MOSFET with datasheet reference CMF20120D. The currents were measured using a Tektronix current probe model TCP-312. The oscilloscope used was a Lecroy Wavesurfer 104MXs-B.

As it was mentioned in chapter 2, silicon PiN diodes exhibit a characteristic reverse recovery caused by the removal of the stored charge [7]. Over the years, minority carrier lifetime engineering has been used for improving the switching performance of silicon PiN diodes. The selected silicon PiN diode is a fast recovery epitaxial diode, with platinum doped lifetime control [16].

In the case of parallel diodes, if the junction temperature of the chips is different (because of the uneven degradation of the packaging, for example) the impact on the turn-off transient and its implications on its use as TSEP should be studied.

Given the extra inductance added to the circuit in order to be able to modify the temperature of the chips individually, the studies for parallel devices have been conducted at low switching rates, using a gate resistance $R_G^{EXT} = 150$ Ω was selected.

First, the turn-off transients for parallel diodes and equal temperature should be measured and characterised. The temperature of the parallel diodes was adjusted using the external heaters as it was done in the case of the forward voltage in section 4.2.1. By allowing sufficient time to reach steady-state, it can be assumed that the junction and case temperatures are equal. The characterisation results are shown in Figure 4.16 and Figure 4.17, for parallel silicon PiN diodes and parallel SiC Schottky diodes respectively, where the measured diode current I_D is the total current $I_{D1} + I_{D2}$, as identified in Figure 4.15.

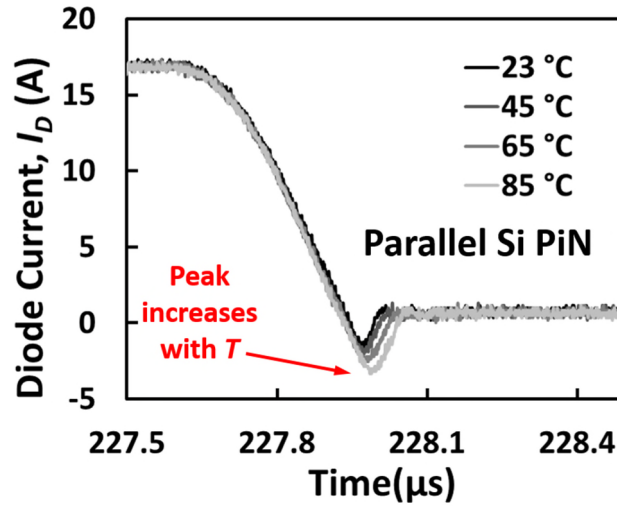


Figure 4.16 Turn-off characteristics of the parallel Si PiN diodes at different temperatures

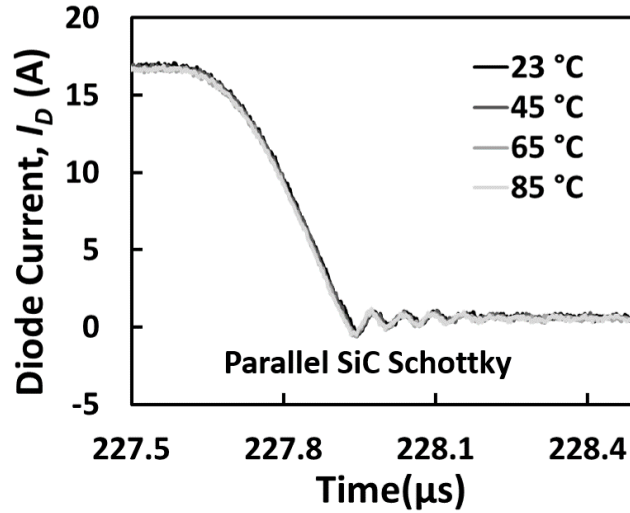


Figure 4.17 Turn-off characteristics of the parallel SiC Schottky diodes at different temperatures

In the case of the parallel Si PiN diodes, as the results in Figure 4.16 show, the effect of the effect of temperature on the reverse recovery is clearly identified with an increased peak recovery current. However, in the case of a SiC Schottky the temperature has no noteworthy impact on the turn-off characteristics, as shown in Figure 4.17.

The next step is the evaluation of the impact of the impact of the temperature imbalance between the parallel chips. This has been studied by adjusting the operating temperature of one of the devices from ambient to 100 °C, while the other was kept at ambient temperature.

The measured turn-off current transients for the parallel Si PiN diodes and SiC Schottky diodes with temperature imbalance between chips are shown in Figure 4.18 and Figure 4.19 respectively. The current shown in these figures is the total current $I_D = I_{D1} + I_{D2}$, as identified before.

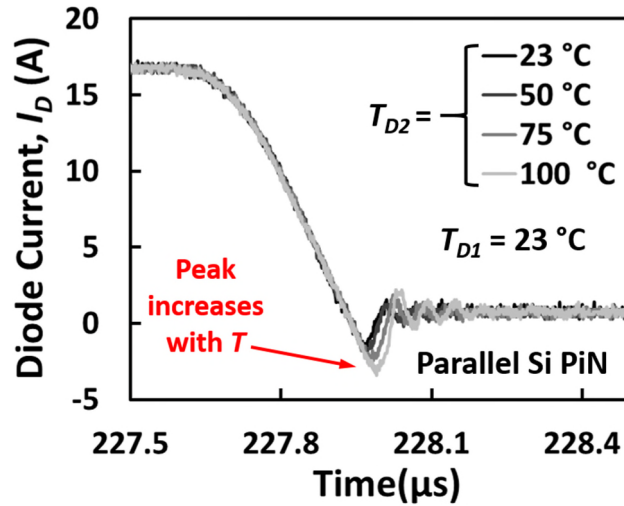


Figure 4.18 Turn-off characteristics of the parallel Si PiN diodes, for temperature imbalance between chips

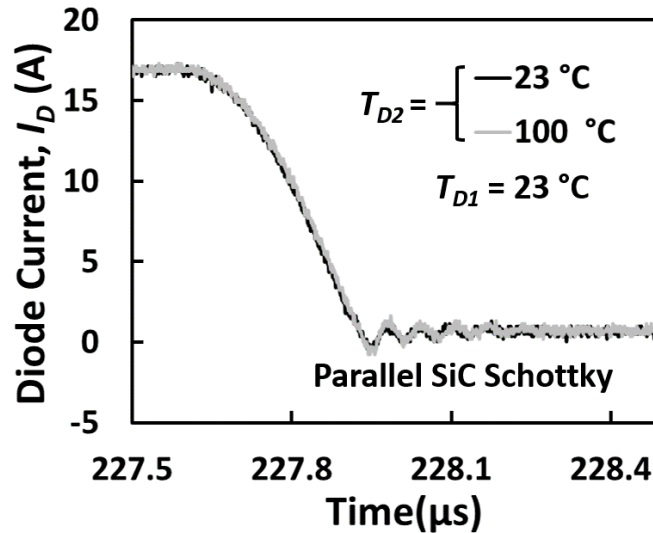


Figure 4.19 Turn-off characteristics of the parallel SiC Schottky diodes, for temperature imbalance between chips

In the case of the parallel SiC Schottky, it can be observed that the temperature imbalance has no visible influence on the turn-off characteristics of the total current. However, in the case of the PiN diode, the peak reverse recovery clearly increases with temperature.

The peak reverse recovery of the parallel silicon PiN diodes has been measured for both the calibration, Figure 4.16, and the imbalance case, Figure 4.18. Table 4-IV shows the measured peak reverse recovery currents for the calibration, hence both chips have the same temperature, and Table 4-V shows the measured peak reverse recovery the imbalanced scenario, indicating the individual chip temperatures as well as the average temperature of the chips. The temperatures were measured using a thermocouple connected to a digital thermometer model KM340 from Comark.

Table 4-IV Measured peak reverse recovery current for parallel PiN diodes with the same temperature (Calibration)

T_{D1} (°C)	T_{D2} (°C)	Peak Reverse Recovery (A)
24	24	-1.730
45	45	-2.050
65	65	-2.530
89	89	-3.329

Table 4-V Measured peak reverse recovery current for parallel PiN diodes with temperature imbalance

T_{D1} (°C)	T_{D2} (°C)	Average Temperature (°C)	Peak Reverse Recovery (A)
23	23	23.0	-1.639
23	50	36.5	-1.959
23	75	49.0	-2.759
23	100	61.5	-3.399

Figure 4.20 shows the normalised peak reverse recovery for the calibration, where both chips have the same temperature, and the diodes with temperature imbalance, calculated using the values from Table 4-IV and Table 4-V. For the imbalanced diodes, the normalised value of the peak reverse recovery current has been plotted as a function

of both the peak temperature (determined by the hotter chip) and the average temperature of the diodes.

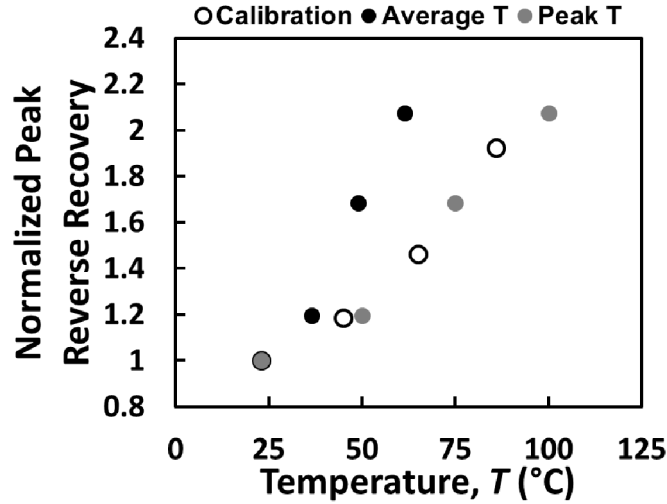


Figure 4.20 Normalised peak reverse recovery current for the parallel Si PiN diodes. Calibration and temperature imbalance between chips

Analysing Figure 4.20, it can be clearly identified that the reverse recovery is determined by the chip with a higher temperature, therefore the reverse recovery as a TSEP would be a suitable indicator of the maximum temperature in the case of parallel PiN diodes.

During the double pulse tests used for the reverse recovery evaluation, the current distribution between the diodes was also measured and characterised. Figure 4.21 shows the current through the hotter diode in for parallel Si PiN diodes with temperature imbalance while Figure 4.22 shows the same characterisation for parallel SiC Schottky diodes. By comparing Figure 4.18 and Figure 4.21, it is clearly observed that the hotter device determines the turn-off transient of the parallel combination of silicon PiN diodes.

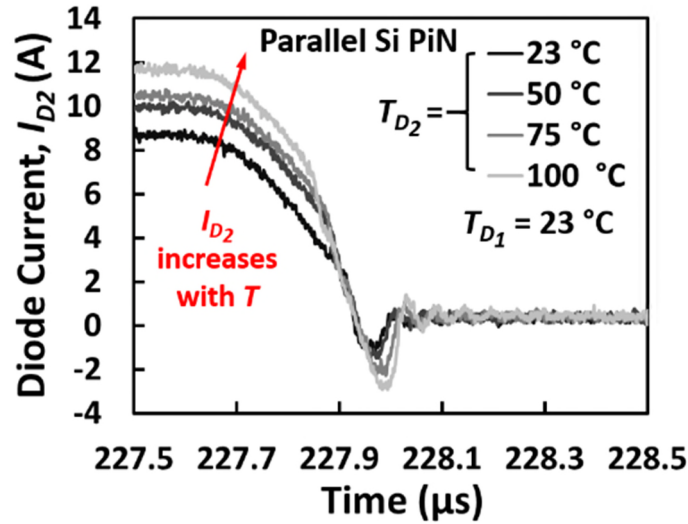


Figure 4.21 Turn-off transient of the hotter chip for parallel Si PiN diodes with temperature imbalance

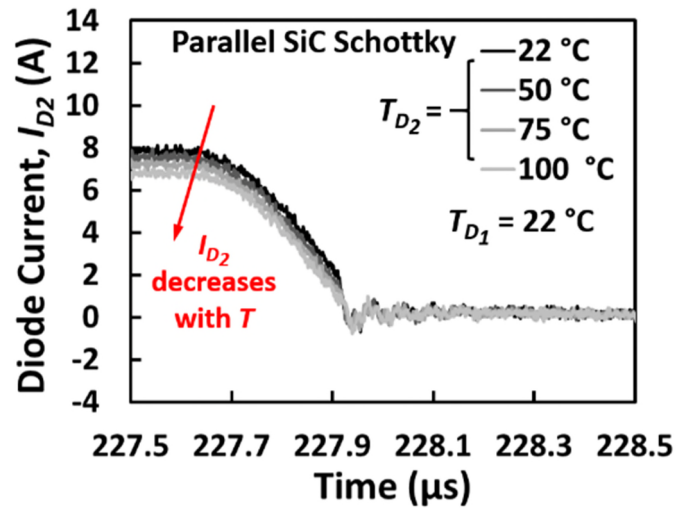


Figure 4.22 Turn-off transient of the hotter chip for parallel SiC Schottky diodes with temperature imbalance

As it was shown in previously in section 4.2.1, the temperature imbalance affects the current distribution of the sensing current, which is below the ZTC point for both Si PiN diodes and SiC Schottky diodes. In the case of Si PiN diodes, the usually higher ZTC point causes that the hotter device to conduct more current compared to a SiC Schottky diode, which has a lower ZTC, meaning that the hotter device will conduct less current in the case of temperature imbalance [17].

This phenomenon is observed for the diode current in the case of the double pulse tests, as the results in Figure 4.21 and Figure 4.22 show. In the case of the parallel PiN diodes, the diode current is below the ZTC and it is clearly observed how the current through the hotter diode increases, however, for the parallel SiC Schottky diodes, the current is above the ZTC and the current through the hotter device decreases. Hence, the current the current distribution could also be an indicator of unequal junction temperature, as the presented results indicate.

The current distribution does not only depend on temperature. Changes in the stray resistances due to electrical degradation of the packaging (for example wire bond lift off) can also affect the current distribution. The current distribution will be studied in chapter 5 for multichip press-pack modules, as an indicator of the health of the module.

4.3 Impact of the gate driver voltage on TSEPs

In the previous chapter, the turn-on switching rate of the drain current dI_{DS}/dt was shown to increase with temperature and was thus identified as a potential TSEP. Due to the impact of parasitic inductance under high dI/dt conditions, the temperature sensitivity was shown to improve when the SiC MOSFET was driven at slower switching speeds. However, since the advantages of SiC are best expedited when driven at high switching speeds, the ability to use the temperature sensitivity of the current switching rate without sacrificing the switching performance appears to be a critical challenge.

As it has been described in chapters 2 and 3 of this thesis, the use of temperature sensitive electrical parameters (TSEPs) is a technique widely used for identifying the junction temperature of power semiconductors. Condition monitoring strategies based on junction temperature identification can be used for assessing ageing damage, improving the lifetime of a power module or setting operational constraints. To this end, the use of advanced intelligent gate drivers [18], capable to momentarily implementing customised switching pulses as part of a condition monitoring strategy can be a significant advantage. A diagnostic pulse can be designed to maximise the temperature sensitivity of a determined TSEP of the device during the junction temperature evaluation, including performing multiple measurements for minimising ambient noise. Since this diagnostic

sequence is used occasionally for condition monitoring, normal operation with low losses and high switching speeds is unperturbed.

This section of the thesis evaluates how the gate driver voltage (V_{GG}) of SiC MOSFETs can be used to maximise the temperature sensitivity of parameters like the on-state resistance R_{DS-ON} or the switching rate of the drain current dI_{DS}/dt of SiC power MOSFETs for a more effective junction temperature identification. The information generated in this chapter can be used for the development of condition monitoring strategies in SiC devices/modules in the future.

4.3.1 Components of a power MOSFET on-state resistance

The on-state resistance of a MOSFET (R_{DS-ON}) is the resistance between the drain and the source terminals of a MOSFET when it is in switched on. Figure 4.23 shows the schematic of a vertically diffused power MOSFET (VD-MOSFET) as well as a trench MOSFET, where the various parasitic resistances that contribute to the total on-state resistance are identified [7].

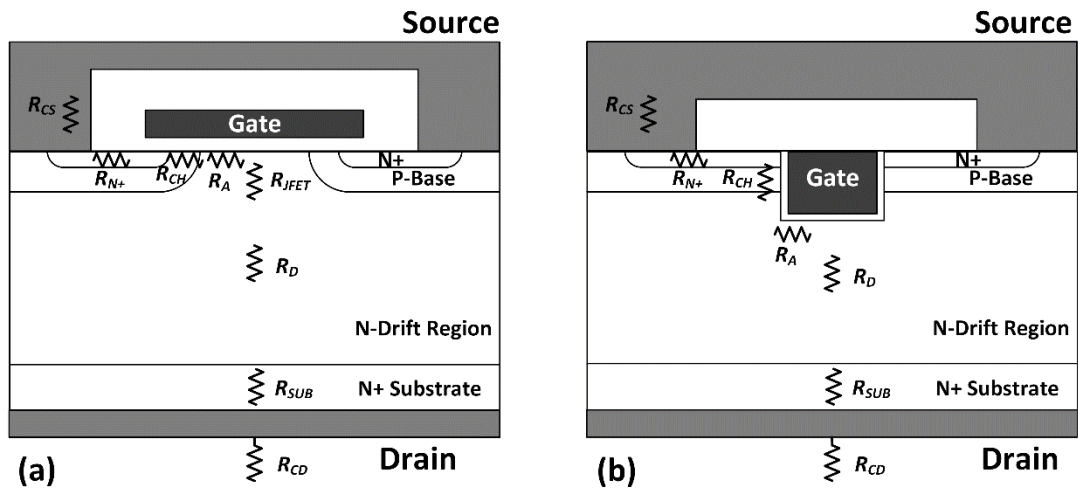


Figure 4.23 (a) Schematic of a VD-MOSFET (b) Schematic of a trench MOSFET. Adapted from [7]

These parasitic resistances include the source contact resistance (R_{CS}) resulting from the finite conductivity of the silicide formed between the source aluminium metal and the N+ doped source region. The source contact resistance is common to VD-MOSFETs and Trench MOSFETs and can be reduced by optimising the silicidation

process (formation of ohmic metal-semiconductor terminal contacts) in the fabrication of power devices. Next in the current path within the MOSFET is the resistance of the N+ doped source region (R_{N+}) determined by the length and sheet resistance of the N+ diffusion.

The channel resistance (R_{CH}), which is the result of the finite conductivity of the inverted channel. The channel resistance dominates the total on-state resistance in very low voltage power MOSFETs and logic devices since there is little or no voltage blocking drift layer. The channel resistance will depend on the threshold voltage, oxide thickness, channel mobility, MOSFET gate width and the channel length (between the source and the drain). In low voltage devices, the channel length is scaled to reduce this resistance. The specific channel resistance of a MOSFET cell $R_{CH,sp}$ is given by equation (4.1) [7], where L_{CH} is the length of the channel. W_{cell} the width of the cell, C_{OX} is the gate oxide capacitance density, μ_{ni} the channel mobility, V_G the gate voltage and V_{TH} the threshold voltage.

$$R_{CH,SP} = \frac{L_{CH}W_{cell}}{2\mu_{ni}C_{OX}(V_G - V_{TH})} \quad (4.1)$$

After the channel resistance is the accumulation layer resistance (R_A) which is formed in the distance between the edge of the p-well and JFET region where the electrons change direction from lateral drift to vertical drift. The accumulation resistance depends on the geometry of the MOSFET and is formed in the N-drift layer underneath the gate dielectric.

Next is the JFET resistance (R_{JFET}), which exists in VD-MOSFETs but not in trench MOSFETs because the channel current flow path in trench MOSFETs eliminates the JFET effect [7, 19]. As a result, trench MOSFET devices have lower on-state resistances compared to VD-MOSFETs in low voltage power MOSFETs where the channel resistance is a considerable fraction of the total resistance and the drift layer resistance is not important. This is usually the case in low voltage high current automotive MOSFETs. The JFET resistance has a positive coefficient with temperature [20, 21].

After the JFET resistance is the drift layer resistance (R_D) which is the most critical resistance in high voltage devices where thick layers are used for voltage blocking. This resistance is independent of the channel architecture (VD-MOSFET vs Trench MOSFET)

and increases with the voltage rating of the power device. This resistance is reduced in SiC power devices because of the thinner voltage blocking epitaxial layers used as a result of the higher critical electric field enabled by the wide bandgap [22]. R_D will be strongly affected by the thickness of the drift region as well as the effective drift mobility of electrons. Unlike the channel resistance (R_{CH}), the temperature coefficient of R_D is positive since mobility degradation is the only temperature dependent parameter that determines R_{DRIFT} [20, 21]. Because the drift layer resistance is smaller for medium voltage (between 600V and 1200 V) SiC power devices compared to silicon devices, the contribution of the channel resistance becomes important.

After the drift resistance is the substrate resistance (R_{SUB}) which results from the finite conductivity of the n+ doping drain region. This resistance is independent of the channel architecture and is considered negligible compared to the drift resistance and the channel resistance in medium and high voltage power MOSFETs. The drain contact resistance (R_{CD}), which similar to the source contact resistance, is formed by the ohmic contact formed between the drain metal and the drain terminal of the device. It can be reduced by optimizing the fabrication process flow. Again, this drain contact resistance is independent of the channel architecture and in medium and high voltage power MOSFETs, it is not as critical as the channel and drift layer resistances. The total on-state resistance of a VD MOSFET can be written as:

$$R_{DS-ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \quad (4.2)$$

In modern power VD-MOSFETs, the critical resistances are the channel resistance (dominant in low voltage devices) and the drift resistance (dominant in high voltage devices). Considering the main contributors the on-state resistance [7, 20, 21], for medium voltage SiC VD-MOSFETs, equation (4.2) can be rewritten as

$$R_{DS-ON} \approx R_{CH} + R_{JFET} + R_D \quad (4.3)$$

In the case of trench MOSFETs, equation (4.3) can be further simplified to

$$R_{DS-ON} \approx R_{CH} + R_D \quad (4.4)$$

The temperature coefficient of R_{CH} depends on a combination of the threshold voltage (which has a negative TC and reduces R_{CH}), the effective mobility (which has a negative TC and increases R_{CH}) and the gate voltage applied to the device. The other components identified in equation (4.3) and (4.4) have a positive temperature coefficient.

4.3.2 Impact of the gate driver voltage on the temperature sensitivity of R_{DS-ON}

As it has been already presented in chapter 3, depending on the technology and the material, the on-state resistance of a MOSFET will show different trends with temperature. In silicon MOSFETs where R_D is the dominant component of R_{DS-ON} , the temperature coefficient (TC) is always strongly positive since R_{CH} is not critical. However, in devices where the R_{CH} is a larger component of the total R_{DS-ON} (like 650 V SiC trench power MOSFETs), the TC of R_{DS-ON} shows both positive and negative temperature coefficient depending on the gate-source voltage (V_{GS}), with a high gate voltage required for obtaining a low resistance value. This is a well known phenomenon and it is one of the reasons why SiC MOSFETs require a high gate voltage in order to obtain a low on-state resistance compared with silicon MOSFETs [20, 21], as well as avoiding a negative temperature coefficient, which can cause thermal runaway in case of paralleled devices.

In addition to the intrinsic device resistance, which is modelled by equation (4.2), there are parasitic resistances which add to the total resistance of the packaged MOSFET chip. These include the wirebond resistances, metallization, solder, mounting substrate, etc., which will add to the total resistive path within the packaging, as shown in Figure 4.24.

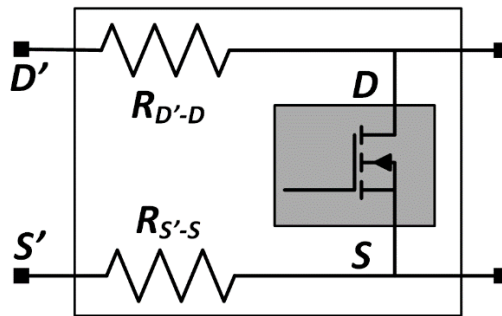


Figure 4.24 Impact of stray resistances on the measured on-state resistance of a packaged MOSFET and kelvin connection

It is important to mention that a recent packaging trend consists in the addition of a kelvin connection so as to minimise the impact of the stray inductance on the switching performances. The use of this additional terminal for evaluating bond-wire degradation and chip degradation has been demonstrated in [23] by characterising the on-state voltage.

Using the test setup for the characterisation of static TSEPs described in chapter 2, the on-state resistance of different power MOSFETs has been characterised. The operating temperature of the devices was set using the heaters described in chapter 2. The on-state resistance was characterised at low currents by injecting a current of 50 mA, measuring the on-state voltage for different gate voltages. A digital multimeter Hameg model HMC8012 was used for measuring the on-state voltage and a power supply model EL302RT from TTI was used for generating the sensing current, measured using a digital multimeter Fluke 175.

Figure 4.25 presents the measured on-state resistance of a 1200 V /24 A SiC MOSFET with datasheet CMF10120D from Cree/Wolfspeed, at different V_{GS} voltages as a function of temperature.

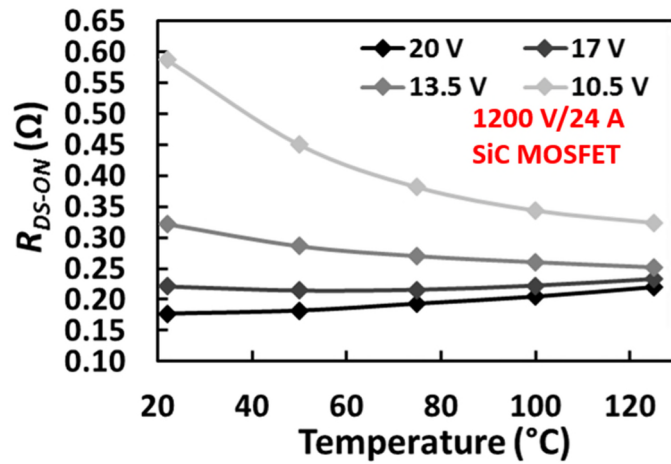


Figure 4.25 Measured R_{DS-ON} of a 1200 V/24 A SiC MOSFET as a function of temperature, for different V_{GS} voltages

From the measurements presented in Figure 4.25 it is observed that at low V_{GS} values the temperature coefficient of R_{DS-ON} is negative and becomes positive as V_{GS} increases. The impact of the gate voltage on the on-state resistance is clearly observed on Figure 4.26, where the normalised on-state resistance values are shown as a function of temperature, with a clear NTC at low V_{GS} and a clear PTC at high V_{GS} .

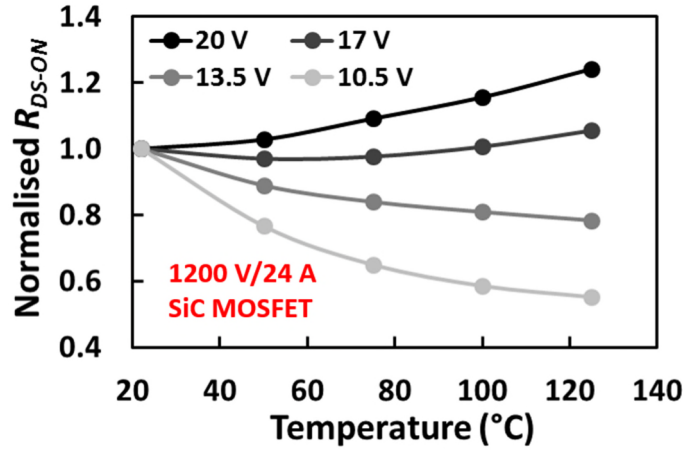


Figure 4.26 Normalised R_{DS-ON} of a 1200 V/24 A SiC MOSFET as a function of temperature, for different V_{GS} voltages

As it was mentioned before, this characteristic is peculiar to medium-high voltage SiC MOSFETs, where the channel resistance is a considerable fraction of the total resistance, unlike silicon MOSFETs where the voltage blocking drift region dominates the total on-state resistance. In the case of SiC MOSFETs the resistance of the drift region is smaller since significantly thinner layers are required for blocking high voltages as a result of the higher critical electric field in silicon carbide.

Figure 4.27(a) shows the measured on-state resistance values for the 1200 V/24 A SiC MOSFET, as a function of V_{GS} for two temperatures, namely 22 °C and 125 °C, while Figure 4.27(b) shows a similar plot for a 1200 V/20 A Si MOSFET from IXYS, with datasheet reference IXFX20N120P. The gate voltages used ranged from 10.5 V to 20 V for both the SiC and Si MOSFET. By comparing the plots for the two devices, it can be seen that the temperature coefficient of the R_{DS-ON} in the SiC MOSFET is influenced by V_{GS} since it goes from negative to positive as V_{GS} is increased, whereas for the silicon MOSFET, the temperature coefficient of R_{DS-ON} is always positive. Figure 4.28 shows the measured R_{DS-ON} of a 900 V/15 A Si COOLMOS from Infineon with datasheet reference IPW90R340C3. As in the case of the Si MOSFET characteristics shown in Figure 4.27(b), the on-state resistance has a PTC for the gate voltages evaluated. By comparing the measured R_{DS-ON} values, it is also observed that the on-state resistance of the SiC MOSFET is lower than the on-state resistance of the Si MOSFET and the COOLMOS, especially at high temperatures.

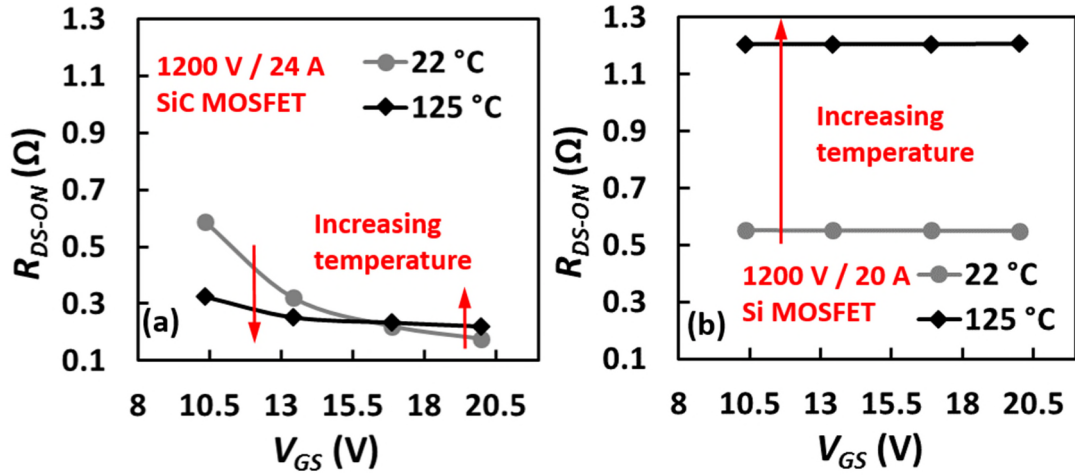


Figure 4.27 Measured R_{DS-ON} as a function of the V_{GS} voltage at 22 °C and 125 °C.
(a) 1200 V/24 A SiC MOSFET (b) 1200 V/20 A Si MOSFET

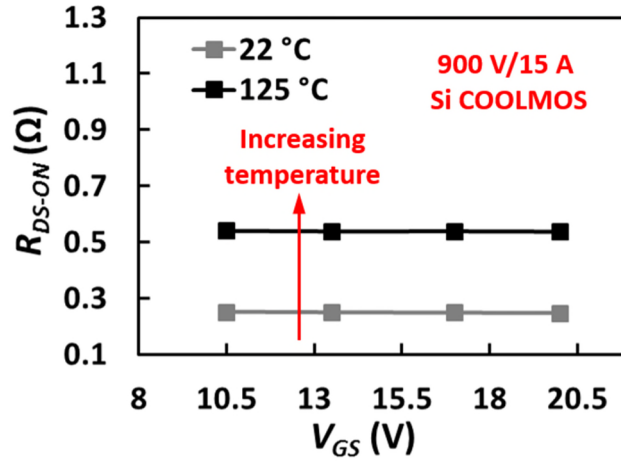


Figure 4.28 Measured R_{DS-ON} as a function of the V_{GS} voltage at 22 °C and 125 °C of a 900 V/15 A Si COOLMOS

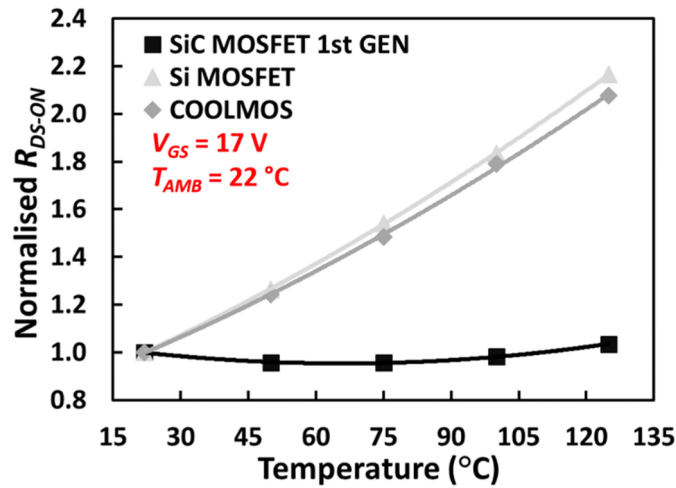
There are methods which use the on-state resistance of a MOSFET as TSEP, like [24], where the authors analyse the temperature sensitivity of Si COOLMOS devices and [23, 25], where the on-state resistance of SiC MOSFETs is used as TSEP. From the results presented in Figure 4.27 and Figure 4.28, it can be observed that in the range of 10 to 20 V the gate voltage has no noteworthy impact on the temperature sensitivity of the on-state resistance. However, in the case of the SiC MOSFET, as the results on Figure 4.27(a) indicate, the gate voltage used would have a substantial impact on the temperature sensitivity of the on-state resistance.

The temperature sensitivity for both the Si MOSFET and COOLMOS is shown in Table 4-VI, for temperatures between 22 °C and 125 °C.

Table 4-VI Temperature sensitivity of the on-state resistance for a 1200 V/20 A Si MOSFET and a 900 V/15 A Si COOLMOS for different gate voltages

Si MOSFET 1200 V/20 A			Si COOLMOS 900 V/15 A		
V_{GS} (V)	dR_{DS-ON}/dT (m Ω /°C)	Variation (%)	V_{GS} (V)	dR_{DS-ON}/dT (m Ω /°C)	Variation (%)
10.5	6.35	118.52	10.5	2.80	114.27
13.5	6.36	118.96	13.5	2.80	115.02
17	6.36	119.08	17	2.81	116.13
20	6.38	119.45	20	2.80	116.26

As the results in Table 4-VI show, the sensitivity of the on-state resistance is good for both silicon devices, with an increase of the nominal resistance of more than 115 % and temperature sensitivities of 6.36 m Ω /°C and 2.80 m Ω /°C for the Si MOSFET and the Si COOLMOS respectively. The normalised on-state resistance as a function of temperature shows a good linear response with temperature for both devices, as the results in Figure 4.29 show. However, in the case of SiC for a gate voltage of 17 V, as it has been shown previously, the response of the on-state resistance has both NTC and PTC zones and it is not linear.

**Figure 4.29 Normalised R_{DS-ON} as a function of temperature for a 900 V/15 A Si COOLMOS, 1200 V/20 A Si MOSFET and a 1200 V/24 A SiC MOSFET. $V_{GS}=17$ V**

Referring back to Figure 4.25 and Figure 4.27(a), the impact of the gate voltage on the temperature sensitivity of the on-state resistance for the 1200 V/24 A SiC MOSFET has been calculated and it is shown in Table 4-VII.

Table 4-VII Temperature sensitivity of the on-state resistance for a 1200 V/24 A SiC MOSFET for different gate voltages

SiC MOSFET 1200 V/24 A		
V_{GS} (V)	dR_{DS-ON}/dT (m Ω /°C)	Variation (%)
10.5	-2.56	-44.84
13.5	-0.68	-21.64
17	0.12	5.52
20	0.42	24.15

Table 4-VII presents the absolute temperature sensitivity and it is important to remark that the temperature response is not linear, as the results on Figure 4.25 show. However, the absolute temperature sensitivity values are a good indicator of how the gate driver voltage could be used for increasing the temperature sensitivity of the on-state resistance.

For increasing the current rating of the MOSFET, a larger die is required and the nominal on-state resistance will be lower. The impact of the gate voltage on the temperature sensitivity of a 1200 V/42 A from Cree/Wolfspeed, with datasheet reference CMF10120D, was evaluated using the same experimental setup than the previous MOSFETs. Figure 4.30(a) shows the measured on-state resistance as a function of temperature for a series of gate voltages, while Figure 4.30(b) shows the normalised on-state resistance increase.

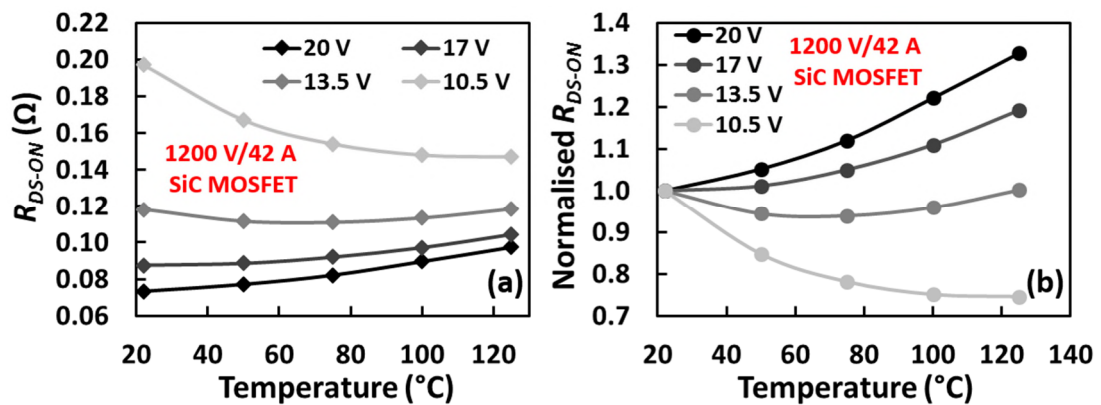


Figure 4.30 (a) Measured R_{DS-ON} of a 1200 V/42 A SiC MOSFET as a function of temperature, for different V_{GS} voltages, (b) Normalised R_{DS-ON} of a 1200 V/42 A SiC MOSFET as a function of temperature, for different V_{GS} voltages

The on-state resistance of the 1200 V/42 A SiC MOSFET as a function of the gate voltage is presented in Figure 4.31, for two temperatures (22 °C and 125 °C). The existence of a ZTC point is observed and comparing with the 1200 V/24 A device, as shown in Figure 4.27(a), it is clearly observed that its value is lower, indicating a different contribution of the different resistances of the MOSFET due to the change of the area of the device.

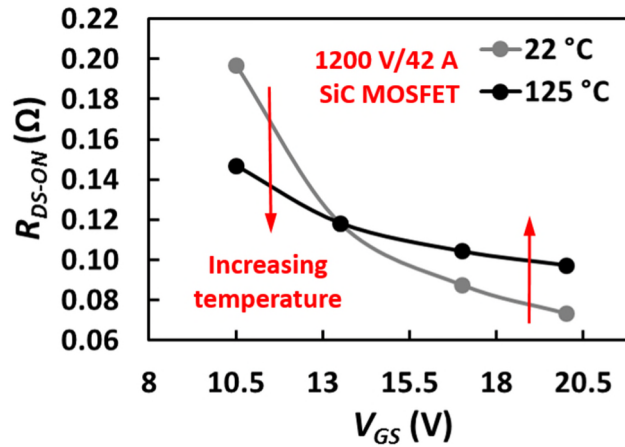


Figure 4.31 Measured R_{DS-ON} as a function of the V_{GS} voltage at 22 °C and 125 °C of a 1200 V/42 A SiC MOSFET

The impact of the gate voltage on the temperature sensitivity of the on-state resistance for the 1200 V/42 A SiC MOSFET has been calculated from the measurements presented in Figure 4.30 and it is shown in Table 4-VIII.

Table 4-VIII Temperature sensitivity of the on-state resistance for a 1200 V/42 A SiC MOSFET for different gate voltages

SiC MOSFET 1200 V/42 A		
V_{GS} (V)	dR_{DS-ON}/dT (mΩ/°C)	Variation (%)
10.5	-0.49	-25.38
13.5	~ 0.002	0.17
17	0.16	19.18
20	0.23	32.70

As in the case of the 1200 V/24 A SiC MOSFET, the response is not linear and the presented sensitivities are the absolute ones. For a gate voltage of 13.5 V, the device presents a reduced temperature sensitivity, with both negative and positive temperature

coefficients. From the temperature sensitivities presented in Table 4-VIII, an interesting observation in the case of the 1200 V/42 A SiC MOSFET is that for a gate voltage of 20 V the increase of resistance in percentage is higher (32.70 % compared with -25.38 %), however the temperature sensitivity is more than double for a gate voltage of 10.5 V (-0.49 mΩ/°C compared with 0.23 mΩ/°C).

Improvements in the channel resistance [20] of the second generation of SiC MOSFETs by Cree/Wolfspeed result in a better positive temperature coefficient compared with their previous generation of SiC MOSFETs (which was characterised previously in Figure 4.25 and Figure 4.26). The on-state resistance of a second generation 1200 V/19 A SiC MOSFET from Cree/Wolfspeed is shown in Figure 4.32. For this particular SiC MOSFET, reducing the gate voltage down to 10.5 V would not have an impact on the temperature sensitivity of the on-state resistance, as the results on Figure 4.33 show.

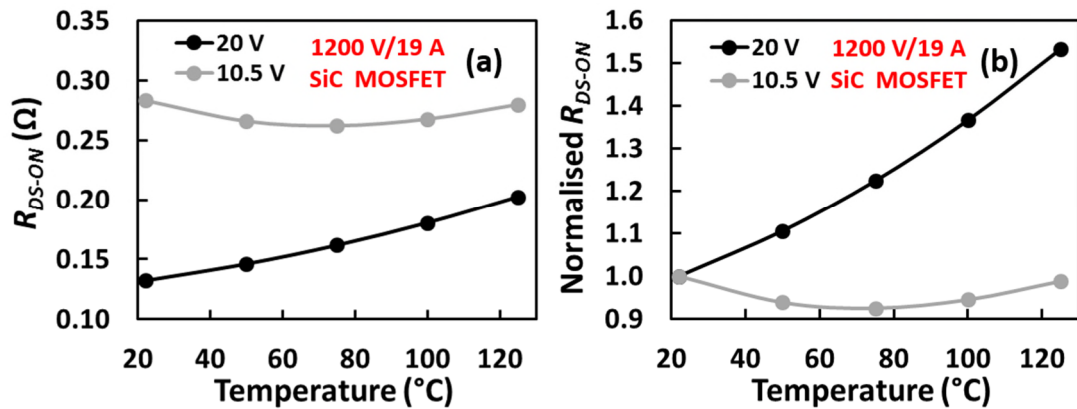


Figure 4.32 (a) Measured R_{DS-ON} of a 1200 V/19 A SiC MOSFET 2G as a function of temperature, for different V_{GS} voltages, (b) Normalised R_{DS-ON} of a 1200 V/19 A SiC MOSFET 2G as a function of temperature, for different V_{GS} voltages

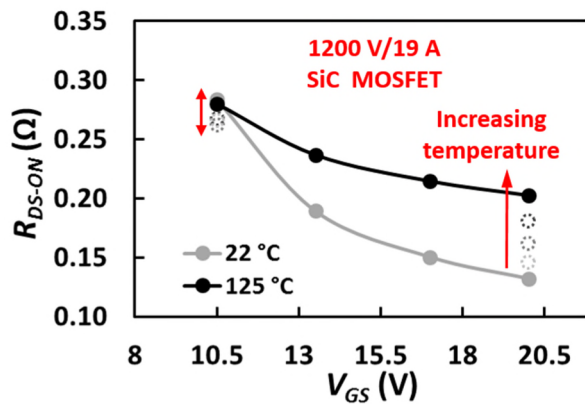


Figure 4.33 Measured R_{DS-ON} as a function of the V_{GS} voltage at 22 °C and 125 °C of a 1200 V/19 A SiC MOSFET 2G

Recently, the emergence of SiC Trench MOSFETs devices seems to be the technology adopted by different manufacturers [26-29]. Trench MOSFETs have a lower input capacitance and a lower on-state resistance for the same device area compared with a planar MOSFET [30, 31]. This reduction of the on-state resistance appears as a result of the reduced channel resistance together with the elimination of the JFET region of the MOSFET [7, 29, 31], as can be seen by comparing equations (4.3) and (4.4).

The on-state resistance of a 650 V/39 A SiC Trench MOSFET from Rohm with datasheet reference SCT3060AL has been characterised at different temperatures for gate voltages of 20 V and 10.5 V using the using the same experimental setup than the previous MOSFETs in this chapter. The results are presented in Figure 4.34, with the measured on-state resistance as a function of temperature shown in Figure 4.34(a) and the normalised values in Figure 4.34(b).

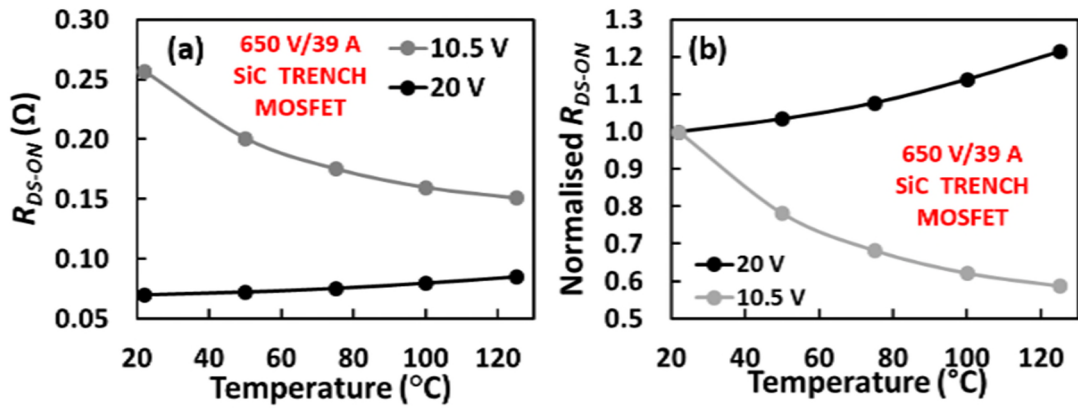


Figure 4.34 (a) Measured R_{DS-ON} of a 650 V/39 A SiC Trench MOSFET as a function of temperature, for different V_{GS} voltages, (b) Normalised R_{DS-ON} of a 650 V/39 A SiC Trench MOSFET as a function of temperature, for different V_{GS} voltages

As in the case of the previously evaluated planar SiC MOSFETs, the temperature coefficient is positive for high gate voltages and negative if the gate voltage is reduced. In the case of the gate voltage of 20 V, the response can be considered linear, while for a gate voltage of 10.5 V it is clearly not linear.

Table 4-IX shows the temperature sensitivities and it is clearly observed how reducing the gate voltage would increase the effectivity of the on-state resistance as TSEP, with temperature sensitivity around seven times higher.

Table 4-IX Temperature sensitivity of the on-state resistance for a 650V/39 A SiC Trench MOSFET for different gate voltages

SiC MOSFET 650 V/39 A		
V_{GS} (V)	dR_{DS-ON}/dT (mΩ/°C)	Variation (%)
10.5	-1.03	-41.29
20	0.15	21.42

An important consideration about the use of the on-state resistance as TSEP is that the thickness of the different layers of the MOSFET (voltage rating) and the chip area (current rating) define its nominal value. As the presented results in this chapter indicate, the effectiveness of reducing the gate voltage for improving the temperature sensitivity of the on-state resistance should be studied for each MOSFET, especially given the different generations available on the market, including different voltage and current ratings. The differences will affect the contribution of each layer to the total resistance, hence the temperature sensitivity of each model can be completely different. The variability of the on-state resistance for devices of the same technology but different batches should also be studied. Calibration and normalisation techniques can help with this issue.

Another important remark is that in the case of power modules multiple chips are connected in parallel for increasing the current capability, as it was shown in section 4.1. If the devices are driven at low V_{GS} values for increasing the temperature sensitivity of R_{DS-ON} , the negative temperature coefficient of the on-state can lead to thermal runaway. However, the higher temperature sensitivity of the on-state resistance at low V_{GS} voltages could be exploited using an intelligent gate driver capable of applying customised occasional switching pulses for junction temperature estimation [18]. The on-state voltage could be characterised at low V_{GS} for a determined sensing cycle, resulting in a higher on-state voltage thereby making the characterisation/measurement easier. Once the sensing cycle is complete, the output voltage of the gate driver can then be adjusted to the normal V_{GS} value, hence limiting the risk of thermal runaway in case of parallel chips and reducing the conduction losses. In addition to the increased temperature sensitivity, the on-state resistance contribution of the MOSFET chip would be higher, compared with

the parasitic resistances of the packaging. Again, this would aid junction temperature sensing.

Using the on-state resistance as TSEP is a method already implemented for condition monitoring [23, 25] and it would benefit from the augmentation of the monitored parameter presented in this thesis, since increasing the nominal on-state resistance will increase the measured on-state voltage. In [32], a gate driver which can modify the output voltage and the output resistance was presented for achieving active thermal control.

4.3.3 *Impact of the gate driver voltage on the temperature sensitivity of the switching rate*

The switching rate of the drain current during turn-on (dI_{DS}/dt) was presented as a potential TSEP for SiC MOSFETs in chapter 3 and it was shown that its temperature sensitivity is improved when the magnitude of the switching rate is reduced.

It was shown that the temperature sensitivity of the turn-on transient is determined by the negative temperature coefficient of the threshold voltage (V_{TH}). For both Si and SiC MOSFETs, the impact of the lower threshold voltage with temperature is manifested in the forward time shift of the current transient defined by equation (4.5), where it is assumed that the charging of the input capacitance C_{ISS} starts at $t=0$. The value t_{TH} defines the point in time when the gate voltage V_{GS} reaches the threshold voltage. R_G is the total gate resistance ($R_G=R_G^{INT}+R_G^{EXT}$), C_{ISS} the input capacitance and V_{GG} the output voltage of the gate driver, including the internal drop in the gate driver circuit.

$$t_{TH} = R_G C_{ISS} \ln \left(\frac{V_{GG}}{V_{GG} - V_{TH}} \right) \quad (4.5)$$

It was also demonstrated that when the SiC MOSFETs are switched at lower rates, hence using a higher R_G^{EXT} , the hindering effect of the parasitic inductances on the temperature sensitivity of the turn-on transient is minimised, obtaining a more apparent temperature sensitivity of the switching rate. Neglecting the impact of the parasitic inductance, the switching rate of the drain current of a MOSFET in saturation is given by

equation (4.6), whereas its temperature dependency modelled by equation (4.7), where β is the gain factor of the MOSFET.

$$\frac{dI_{DS}}{dt} = \beta (V_{GS}(t) - V_{TH}) \frac{dV_{GS}}{dt} \quad (4.6)$$

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{dV_{GS}}{dt} \left(\frac{d\beta}{dT} (V_{GS}(t) - V_{TH}) - \beta \frac{dV_{TH}}{dT} \right) \quad (4.7)$$

The gate-source voltage $V_{GS}(t)$ is given by

$$V_{GS} = V_{GG} \left(1 - e^{-\frac{t}{R_G C_{ISS}}} \right) \quad (4.8)$$

With its derivative

$$\frac{dV_{GS}}{dt} = \frac{V_{GG}}{R_G C_{ISS}} e^{-\frac{t}{R_G C_{ISS}}} \quad (4.9)$$

The transconductance of a MOSFET in saturation given by

$$g_{mS} = \beta (V_{GS}(t) - V_{TH}) \quad (4.10)$$

With its derivative respect temperature given by

$$\frac{dg_{mS}}{dT} = \frac{d\beta}{dT} (V_{GS}(t) - V_{TH}) - \beta \frac{dV_{TH}}{dT} \quad (4.11)$$

Using equation (4.11), equation (4.7) can be rewritten as

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{dV_{GS}}{dt} \frac{dg_{mS}}{dT} \quad (4.12)$$

The impact of the gate driver voltage on temperature dependency of the switching rate can be studied evaluating equation (4.12), which can be divided in two parts. Evaluating the first part, given by equation (4.9), the input capacitance is not affected by temperature [33] and considering the total gate resistance R_G constant (low temperature sensitivity of R_G^{INT} [34] and using a large external gate resistance R_G^{EXT} to minimise the impact of the stray inductances), the temperature would have no impact in this term. According to this, reducing the gate driver voltage causes a reduction on the switching rate, which is a well-known fact.

Equation (4.11) models the second term of the temperature dependency of the switching rate. The temperature affects both β and the V_{TH} in this equation and, as it has been shown in chapter 3, in SiC MOSFETs the negative coefficient of the threshold voltage dominates the reduction of mobility with temperature, which in addition can be considered approximately constant for the range of temperatures evaluated here [35, 36].

For a determined temperature, if the gate voltage is reduced, the value $\frac{d\beta}{dT}(V_{GS}(t) - V_{TH})$ is smaller and the contribution of the negative temperature coefficient of the threshold voltage to the increase of the switching rate is higher. Hence, if the gate voltage is reduced, the temperature sensitivity of the switching rate is increased.

In chapter 3 it was shown that the relative temperature sensitivity is higher for higher rated current devices, hence the 1200V/42A SiC MOSFET from Cree/Wolfspeed with datasheet reference CMF20120D has been selected for the experimental evaluation of the impact of the gate driver supply voltage (V_{GG}) on the temperature sensitivity of the switching rate.

The turn-on transient was studied using the double pulse test setup which was presented in chapter 2, using the small DC heaters presented in the same chapter for defining the operating junction temperature. The temperatures were adjusted from 50 °C to 150 °C, leaving enough time to reach a steady state which allows the assumption of the junction temperature equal to the case temperature. The DC link voltage (V_{DC}) selected for these tests was 600 V, the inductor L of 2 mH and the freewheeling diode was a 1200V/16A SiC Schottky diode with datasheet reference C4D10120A from Cree/Wolfspeed, which is a single chip TO-220 packaged diode.

The turn-on transient was characterised for a set of external gate resistances R_G^{EXT} , namely 47 Ω , 100 Ω and 220 Ω , and a series of gate driver voltages V_{GG} namely 10.5 V, 13.5 V, 17 V and 20 V. The gate voltages were obtained using the gate driver circuit presented in chapter 2, where the supply voltage can be adjusted using a combination of resistors [37].

The captured waveform transients for an external gate resistance $R_G^{EXT}=47 \Omega$ and the different gate voltages are shown in Figure 4.35, whereas the captured waveform transients, for the gate driver voltage of 20 V and the 100 Ω and 220 Ω external gate resistances are shown in Figure 4.36. External gate resistances values of 47 to 220 Ω have been selected to minimise the impact of the stray inductances on the temperature sensitivity of the switching rate, as it was explained in chapter 3.

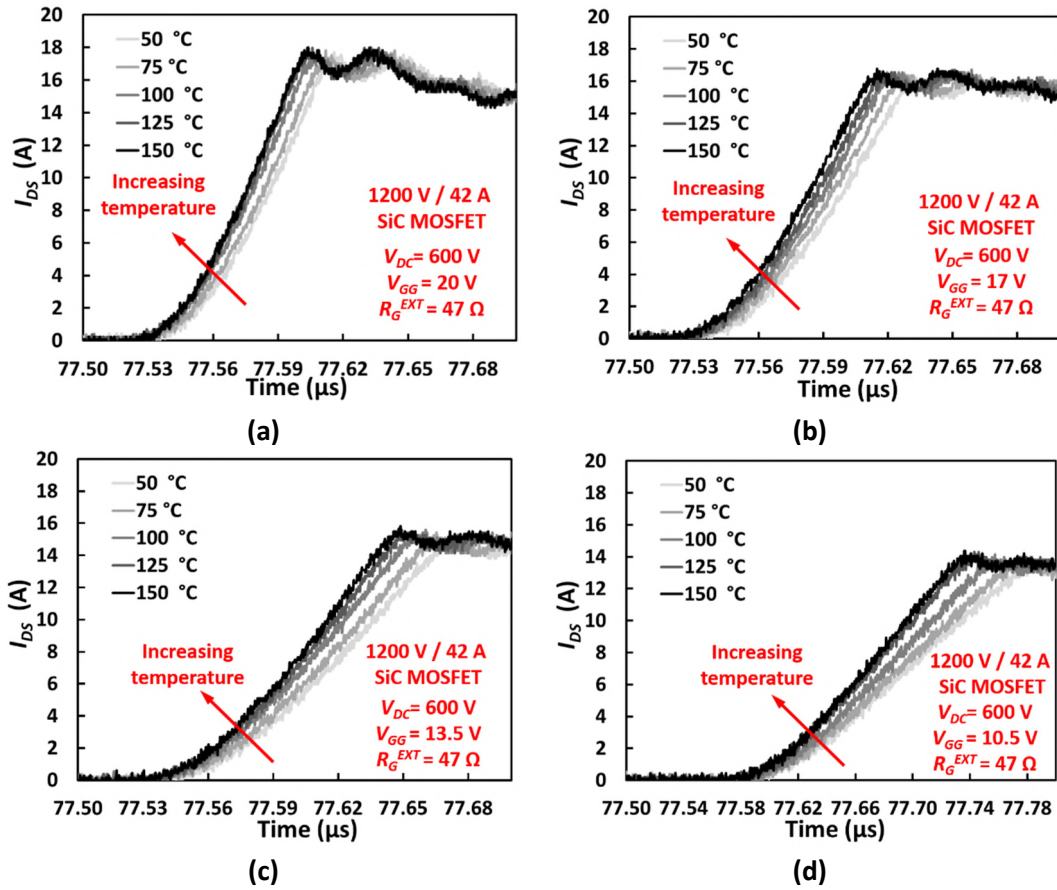


Figure 4.35 Drain-Source current during turn-on of a 1200V/42 A SiC MOSFET. $R_G^{EXT}=47 \Omega$. (a) $V_{GG}=20$ V, (b) $V_{GG}=17$ V, (c) $V_{GG}=13.5$ V, (d) $V_{GG}=10.5$ V

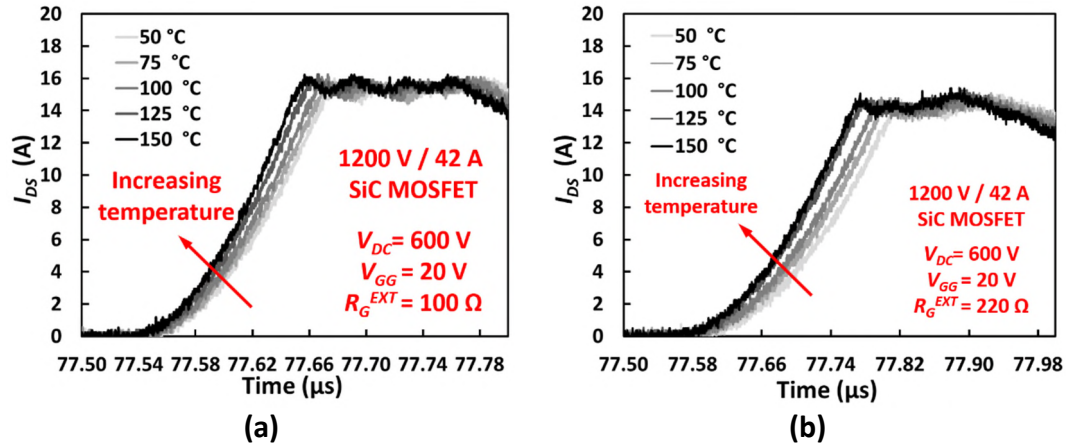


Figure 4.36 Drain-Source current during turn-on of a 1200V/42 A SiC MOSFET. $V_{GG}=20$ V, (a) $R_G^{EXT}=100\ \Omega$, (b) $R_G^{EXT}=220\ \Omega$

In both Figure 4.35 and Figure 4.36 the shift in time of the turn-on transient and the increase of the switching rate of the current with temperature are clearly identified. Moreover, during the initial stages of the turn-on transient, when the value of V_{GS} is low, a higher temperature sensitivity of the switching rate is also observed, especially in Figure 4.36(b), for a gate driver voltage $V_{GG}=20$ V and an external gate resistance $R_G^{EXT}=220\ \Omega$

Using the measured transients, the switching rate has been calculated as the average slope for the set of measurements performed. The calculated values are presented in Figure 4.37 and Figure 4.38. Figure 4.37 presents the switching rate as a function of temperature for the different gate resistances evaluated and a gate driver voltage of 20 V, whereas Figure 4.38 presents the switching rate as a function of temperature for the different gate driver voltages studied and an external gate resistance of 47 Ω

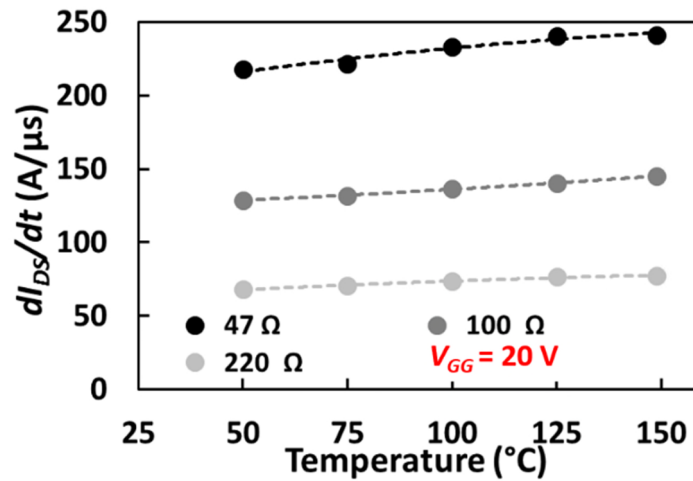


Figure 4.37 Measured dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET as a function of temperature for different gate resistances and $V_{GG}=20$

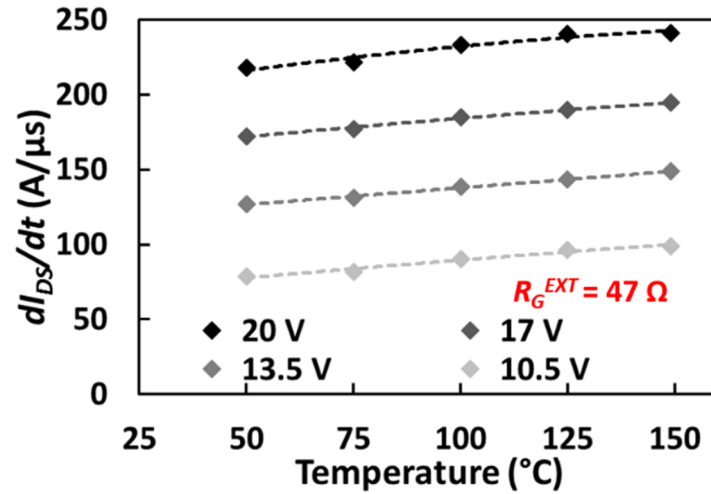


Figure 4.38 Measured dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET as a function of temperature for different gate driver voltages and $R_G^{EXT}=47\ \Omega$

From the results presented in Figure 4.37, it is clearly observed that for a fixed gate driver voltage V_{GG} , when the MOSFET is slowed down by means of increasing the gate resistance, the rate of change of dI_{DS}/dt with temperature decreases. However, evaluating Figure 4.38, if the switching rate is reduced by means of reducing the gate driver voltage, the temperature coefficient of dI_{DS}/dt is approximately constant, with only a slight reduction.

An important distinction must be made between the temperature coefficient of the absolute switching rate and that of the relative switching rate, normalised to a reference value. This can be evaluated using the results shown in Table 4-X, which presents the measured temperature coefficient of dI_{DS}/dt for the evaluated gate driver voltages of 20 V, 17 V, 13.5 V and 10.5 V, using external gate resistances R_G^{EXT} of 47 Ω and 220 Ω . The evaluated temperature range is 50 to 150 $^{\circ}\text{C}$.

Table 4-X Impact of gate driver on the temperature coefficient of the switching rate dI_{DS}/dt and the normalised increase. Temperature range: 50 °C to 150 °C

	Temperature coefficient (A/ μ s·°C)	Normalised Increase (%)
$V_{GG}=20\text{ V}/R_G^{EXT}=47\text{ }\Omega$	0.24	10.9
$V_{GG}=17\text{ V}/R_G^{EXT}=47\text{ }\Omega$	0.22	12.9
$V_{GG}=13.5\text{ V}/R_G^{EXT}=47\text{ }\Omega$	0.22	17.1
$V_{GG}=10.5\text{ V}/R_G^{EXT}=47\text{ }\Omega$	0.20	25.8
$V_{GG}=20\text{ V}/R_G^{EXT}=220\text{ }\Omega$	0.10	13.9
$V_{GG}=17\text{ V}/R_G^{EXT}=220\text{ }\Omega$	0.08	13.8
$V_{GG}=13.5\text{ V}/R_G^{EXT}=220\text{ }\Omega$	0.08	22.0
$V_{GG}=10.5\text{ V}/R_G^{EXT}=220\text{ }\Omega$	0.07	32.3

The results on Table 4-X show that reducing the gate driver voltage V_{GG} from 20 V to 10.5 V causes a slight reduction of the temperature coefficient of the absolute switching rate (in A/ μ s·°C). For an external gate resistance $R_G^{EXT}=47\text{ }\Omega$, the temperature coefficient changes from 0.24 to 0.20 A/ μ s·°C when the gate voltage is reduced. However, the normalised increase from 50 °C to 150 °C increases noticeably, from 10.9 % to 25.8 %. Hence, it can be concluded that reducing the gate voltage increases the temperature sensitivity of the switching rate as TSEP.

Increasing the gate resistance has also an impact on the temperature sensitivity, as it was demonstrated in chapter 3. In terms of the percentage increase, using a gate driver voltage $V_{GG}=20\text{ V}$, for a gate resistance R_G^{EXT} of 220 Ω the switching rate increases by 13.8 % over the temperature range of 50 °C to 150 °C, compared with the increase of 10.9 % when the external gate resistance value R_G^{EXT} is 47 Ω . If the gate drive voltage is 10.5 V, for a gate resistance R_G^{EXT} of 220 Ω , the percentage increase is 32.3 %. However, as shown in Table 4-X, the temperature coefficient is 0.07 A/ μ s·°C. Although the percentage increase of the switching rate with temperature is higher for the lower V_{GG} and high external gate resistance combination, the lower temperature sensitivity of the switching rate will make the measurement more difficult (from the instrumentation perspective) given the reduced temperature sensitivity. This is clearly observed in Figure 4.39, where the switching rates for a gate voltage of 10.5 V are presented for the evaluated external

gate resistances of 47, 100 and 220 Ω , where a better temperature sensitivity (slope) is observed for the gate resistance $R_G^{EXT} = 47 \Omega$.

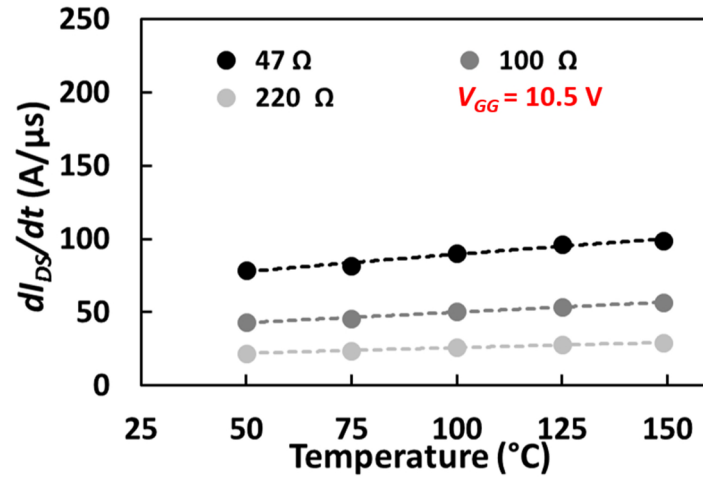


Figure 4.39 Measured dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET as a function of temperature for different gate resistances and $V_{GG}=10.5$

The normalised values of dI_{DS}/dt for gate driver voltages of 10.5 V and 20 V are presented in Figure 4.40, for external gate resistances of 47 Ω and 220 Ω . It is clearly observed how reducing the gate driver voltage has a higher impact on the normalised (relative) switching rate increase with temperature than increasing the gate resistance.

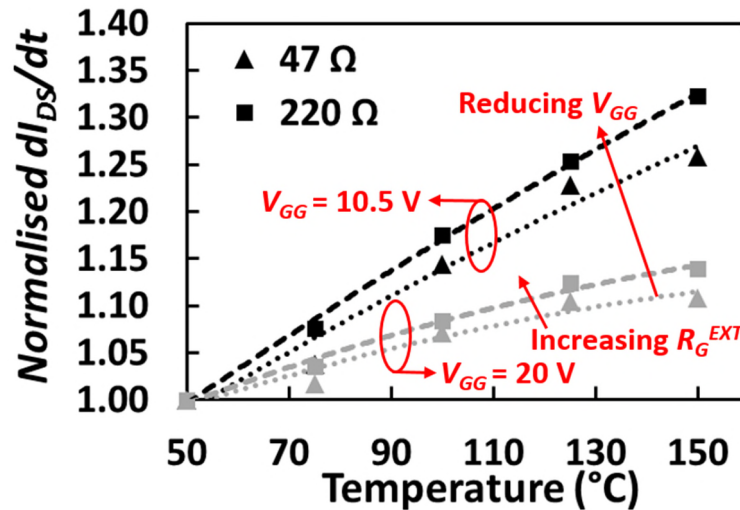


Figure 4.40 Normalised dI_{DS}/dt as a function of temperature, for gate driver voltages of 10.5 and 20 V. $R_G^{EXT} = 47 \Omega$ and 220 Ω

As was already mentioned in section 4.3.2, there are already intelligent gate drivers with the ability to change the output resistance and/or the gate driver supply

voltage [32, 38]. Together with gate drivers with di/dt control proposed for IGBTs [39], this suggests that it is possible to alter the gate driver output for occasional diagnostic pulses needed for online condition monitoring. The characterisation of the TSEP would be performed at low gate driver voltages/large gate resistances and resulting in an augmented temperature sensitivity of the monitored parameter for its characterisation/measurement. The output of the gate driver will be adjusted to a low R_G^{EXT} and high V_{GG} during normal operation, minimising the switching and conduction losses, when the sensing procedure finishes, hence the switching performance of the device during normal operation would not be sacrificed since the device is only slowed down during occasional diagnostic pulses.

The transconductance and the threshold voltage of the MOSFET determine the switching rate. These two parameters are determined by the gate oxide, which has been a source of reliability problems for SiC MOSFETs [40-43]. Hence, additional investigations are required into the impact of decreased oxide integrity on the accuracy of the TSEPs. Also, the impact of having multiple chips in parallel (for increasing the current capability) on the accuracy of the switching rate as TSEP under non-uniform degradation conditions requires further studies.

4.4 Summary

This chapter has used theoretical analysis backed by experimental measurements to investigate the use of TSEPs in the case of parallel connected Si PiN diodes and Si Schottky diodes. The forward voltage at low currents gives the average temperature for both technologies, however as the temperature difference increases, the validity of this global TSEP is limited as the average is not accurate. This is caused by the change in the sensing current distribution. In the case of high temperature imbalance, the current flows mainly through the hotter device, as the sensing point is below the ZTC.

In the case of unequal degradation of the power module, leading to chips with different temperatures, the health state of the module will be determined by the chip with the highest temperature and the average temperature will not be a good condition monitoring indicator. In this case, the local TSEP is a more accurate indicator.

The turn-off transient of parallel connected Si PiN diodes is determined by the hotter device. In this case, the reverse recovery will be a good indicator of the maximum temperature. However, in the case SiC Schottky diodes, the turn off transient is not affected by temperature. The current distribution for parallel connected devices is determined by the ZTC and would be a good indicator of unequal degradation or temperature difference for both Si PiN diodes and SiC Schottky diodes, but it would require the ability to measure currents at chip level.

In this chapter, the impact of the gate driver voltage (V_{GG}) on the temperature sensitivity of the switching rate was also investigated for SiC power MOSFETs. It was shown that the temperature sensitivity can be increased by reducing the gate driver voltage. Measurements showed that the temperature sensitivity of the turn-on switching rate of the SiC MOSFET increased when driven at $V_{GG}=10.5$ V compared to when driven with $V_{GG}=17$ V. This observation is unique to SiC power MOSFETs because unlike silicon MOSFETs, the transconductance increases with temperature during turn-on. In silicon MOSFETs, the negative temperature coefficient of the threshold voltage is counter-balanced by the negative temperature coefficient of the effective mobility, so the saturation transconductance typically reduces with increasing temperature. In SiC MOSFETs, negative temperature coefficient of the threshold voltage dominates the negative temperature coefficient of the effective mobility, hence, the transconductance increases with temperature. This unique property is why the turn-on energy loss reduces as the temperature increases in SiC power MOSFETs. Hence, driving the MOSFET in saturation for longer periods by either using a large gate resistance or by using a smaller V_{GG} , improves the temperature coefficient of the turn-on current switching rate. In the previous chapter, it was shown that switching the device slowly with a large R_G^{EXT} improved the temperature sensitivity since parasitic inductance reduced the temperature sensitivity under high dI/dt conditions.

The knowledge generated in these chapter can be used by experts in gate driver design, to develop condition monitoring strategies capable of altering the gate pulse momentarily for improved use of the TSEPs.

4.5 References

- [1] Cree/Wolfspeed. *CAS100H12AM1 Sales sheet*. Available: https://media.digikey.com/pdf/Data%20Sheets/CREE%20Power/CAS100H12AM1_sales_sheet.pdf (Access: 4/05/2017).
- [2] M. Loboda. *Considerations for designing power electronic devices based on advanced SiC technologies*. Available: <http://www.dowcorning.com/content/publishedlit/11-3382-01.pdf> (Access: 3/05/2017).
- [3] Infineon, "FF1000R17IE4 Datasheet," ed, 2013.
- [4] Semikron. *Influence of parameter distribution and mechanical construction on switching behaviour of parallel IGBT*. Available: <http://www.powerguru.org/influence-of-parameter-distribution-and-mechanical-construction-on-switching-behaviour-of-parallel-igbt/> (Access: 15/06/2017).
- [5] V. K. Sundaramoorthy, E. Bianda, M. Kamel, G. J. Riedel, and I. Nistor, "Online junction temperature estimation for IGBT modules with paralleled semiconductor chips," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, 2014, pp. 1-5.
- [6] M. Denk and M. M. Bakran, "Comparison of U_{CE} - and R_{Gi} -based junction temperature measurement of multichip IGBT power modules," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-11.
- [7] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2008.
- [8] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power Cycle Testing of Power Switches: A Literature Survey," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2465-2473, 2015.
- [9] W. Lai, M. Chen, L. Ran, S. Xu, N. Jiang, X. Wang, *et al.*, "Experimental Investigation on the Effects of Narrow Junction Temperature Cycles on Die-Attach Solder Layer in an IGBT Module," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1431-1441, 2017.
- [10] Mentor. *Mentor Graphics T3ster*. Available: <https://www.mentor.com/products/mechanical/micred/t3ster/> (Access: 26/06/2017).
- [11] M. A. Eleffendi, L. Yang, P. Agyakwa, and C. Mark Johnson, "Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement," *Microelectronics Reliability*, vol. 59, pp. 73-83, 4// 2016.
- [12] D. C. Katsis and J. D. v. Wyk, "Void-induced thermal impedance in power semiconductor modules: some transient temperature effects," *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1239-1246, 2003.
- [13] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2011.

- [14] H. Luo, Y. Chen, W. Li, and X. He, "Online High-Power p-i-n Diode Junction Temperature Extraction With Reverse Recovery Fall Storage Charge," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2558-2567, 2017.
- [15] H. Luo, W. Li, and X. He, "Online high-power P-i-N diode chip temperature extraction and prediction method with maximum recovery current di/dt ," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2395-2404, 2015.
- [16] R. Bürkel and T. Schneider. *Fast Recovery Epitaxial Diodes (FRED) Characteristics - Applications - Examples. IXAN0044*. Available: <http://www.ixys.com/Documents/AppNotes/IXAN0044.pdf> (Access: 5/07/2017).
- [17] J. Hu, O. Alatisse, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Comparative electrothermal analysis between SiC Schottky and silicon PiN diodes: Paralleling and thermal considerations," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1-8.
- [18] B. Ji, W. Cao, and V. Pickert, "State-of-the-art intelligent gate drivers for IGBT power modules - monitoring, control and management at the heart of power converters," in *Control Circuits in Power Electronics: Practical issues in design and implementation*, ed: Institution of Engineering and Technology, 2016, pp. 307-335.
- [19] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, *et al.*, "High performance SiC trench devices with ultra-low ron," in *2011 International Electron Devices Meeting*, 2011, pp. 26.5.1-26.5.3.
- [20] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1478-1483.
- [21] D.-L. DANG, S. GUICHARD, M. Urbain, and S. Raël, "Characterization and modeling of 1200V – 100A N – channel 4H-SiC MOSFET," presented at the Symposium de Genie Electrique, Grenoble, France, 2016.
- [22] Rohm Semiconductor. *SiC Power Devices and Modules Application Note*. Available: http://www.rohm.com/documents/11405/2996964/sic_app-note.pdf (Access: 13/06/2017).
- [23] N. Baker, H. Luo, and F. Iannuzzo, "Simultaneous On-State Voltage and Bond-Wire Resistance Monitoring of Silicon Carbide MOSFETs," *Energies*, vol. 10, no. 3, p. 384, 2017.
- [24] A. Koenig, T. Plum, P. Fidler, and R. W. D. Doncker, "On-line Junction Temperature Measurement of CoolMOS Devices," in *2007 7th International Conference on Power Electronics and Drive Systems*, 2007, pp. 90-95.
- [25] N. Baker, S. Munk-Nielsen, and S. Bęczkowski, "Test setup for long term reliability investigation of Silicon Carbide MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-9.
- [26] Rohm Semiconductor. *300 A SiC Trench MOSFET*. Available: <http://www.rohm.com/web/eu/300a-sic-trench-mosfet> (Access: 17/06/2017).

- [27] Fuji Electric. *1.2 kV SiC Trench MOSFET for All-SiC Modules*. Available: http://www.fujielectric.com/company/research_development/theme/sic_device.html (Access: 17/06/2017).
- [28] Infineon. *Infineon unveils 1200 V Silicon Carbide MOSFET technology for unprecedented efficiency and performance in power conversion design*. Available: <http://www.infineon.com/cms/en/about-infineon/press/market-news/2016/INFIPC201605-053.html> (Access: 8/05/2017).
- [29] Rohm Semiconductor. *The World's First Trench-Type SiC MOSFET*. Available: http://www.rohm.com/web/eu/news-detail?news-title=2015-05-26_ad:-trench-type-sic-mosfet&defaultGroupId=false (Access: 18/06/2017).
- [30] Rohm Semiconductor, "BSM180D12P3C007 Product Bulletin 1200V / 180A Full SiC power module with integrated SiC trench MOSFET," ed, 2016.
- [31] D. Doan, "IS2-4-6 Next-Generation Power SiC Devices for High-Volume Applications " presented at the IEEE Applied Power Electronics Conference APEC 2014, Fort Worth, TX, USA, 2014.
- [32] C. Sintamarean, H. Wang, F. Blaabjerg, and F. Iannuzzo, "The impact of gate-driver parameters variation and device degradation in the PV-inverter lifetime," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2257-2264.
- [33] Rohm Semiconductor. *MOSFET Parasitic Capacitance and Its Temperature Characteristic*. Available: <http://micro.rohm.com/en/techweb/knowledge/si/s-si/03-s-si/4873> (Access: 20/06/2017).
- [34] Y. Lobsiger and J. Kolar, "Voltage, Current and Temperature Measurement Concepts Enabling Intelligent Gate Drives," presented at the ECPE Workshop - Electronics around the power switch: Gate drives, sensors and control Munich 2011.
- [35] M. Hasanuzzaman, S. K. Islam, L. M. Tolbert, and M. T. Alam, "Temperature dependency of MOSFET device characteristics in 4H- and 6H-silicon carbide (SiC)," *Solid-State Electronics*, vol. 48, no. 10–11, pp. 1877-1881, October 2004.
- [36] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 353-363, 2007.
- [37] S. Jahdi, "Analysis of dynamic performance and robustness of silicon and SiC power electronics devices," PhD Thesis, School of Engineering, University of Warwick, 2016.
- [38] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, B. J. Blalock, and X. Wu, "Online junction temperature monitoring using turn-off delay time for silicon carbide power devices," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7.
- [39] Y. Lobsiger and J. W. Kolar, "Closed-Loop di/dt and dv/dt IGBT Gate Driver," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3402-3417, 2015.
- [40] A. Fayyaz and A. Castellazzi, "High temperature pulsed-gate robustness testing of SiC power MOSFETs," *Microelectronics Reliability*, vol. 55, no. 9, pp. 1724-1728, 2015/08/01/ 2015.

- [41] B. J. Nel and S. Perinpanayagam, "A Brief Overview of SiC MOSFET Failure Modes and Design Reliability," *Procedia CIRP*, vol. 59, pp. 280-285, // 2017.
- [42] R. Ouaida, M. Berthou, J. León, X. Perpiñà, S. Oge, P. Brosselard, *et al.*, "Gate Oxide Degradation of SiC MOSFET in Switching Conditions," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1284-1286, 2014.
- [43] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2445-2455, 2015.

5 Evaluation of SiC power devices using pressure contacts

5.1 Introduction - Pressure packaging for Silicon IGBTs

Pressure contacts for power semiconductor devices have historically been used for thyristors deployed in line commutated current source converters (CS-LCC). Since CS-LCCs were the first grid connected converters with significant power handling capability, the architecture of CS-LCC systems became integral to the design of pressure packaging assemblies. CS-LCCs are comprised of series connected thyristors that share the off-state blocking voltage, an arrangement known as thyristor valve stacks. The thyristor valve hall of the Fengxian converter station belonging to the Xiangjiaba Shanghai 800 kV UHVDC is shown in Figure 5.1, where different valve stacks can be observed.



Figure 5.1 Thyristor valve hall of a 800 kV UHVDC converter station [1]

Press-pack thyristors are designed as wafers sandwiched between conducting copper poles, using an intermediate material to match the coefficient of thermal expansion (CTE) of both materials, that also serve as heatsinks. The main benefits of press-pack modules [2] are a compact design, possibility of double side cooling, higher reliability due to the elimination of the solder and wirebonds and a reduced number of interconnections of materials with different CTE. On the other hand, the lack of dielectric

insulation and a more complex mechanical assembly are the major tradeoffs. Figure 5.2(a) shows a 6-inch press-pack thyristor (also called capsule) and its corresponding silicon wafer while Figure 5.2(b) represents the exploded view of a press-pack thyristor [3].

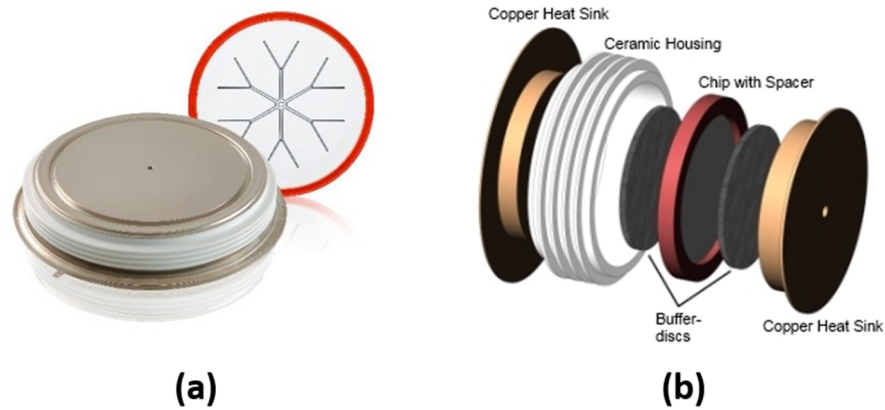


Figure 5.2 (a) 6 inch press-pack thyristor [1] (b) Exploded view of a press-pack thyristor [3]

Failure in short circuit is absolutely critical, hence, the immediate affinity for pressure packaged thyristors in CS-LCC systems. However, in recent decades, there has been a technological migration towards self-commutated voltage source converters (SC-VSC).

The advantages of SC-VSCs are numerous, for example:

- CS-LCCs require synchronous AC systems on both AC terminals of the DC interchange, however SC-VSCs are capable of black-start operation i.e. not only can they operate in weak AC systems, they can act as virtual synchronous generators by synthesizing a balanced set of 3 AC voltages from a DC source.
- Because phase-to-phase commutation in CS-LCCs is initiated by system AC voltage reversal, switching in such systems is done at line frequency which is 50 Hz or 60 Hz. This is because traditional thyristors, known as phase commutated thyristors (PCT) are not capable of self-turn-off, hence, once the PCT is latched, it can only be turned off by voltage reversal from the AC mains. Because switching is limited to the grid frequency, DC and AC side filtering requirements (capacitors for voltage harmonics and reactors for current harmonics) are significantly large and expensive in CS-LCCs. However, in SC-VSCs, switching is performed entirely at the discretion of the controller since the devices are

capable of self-turn off. Examples of devices used in SC-VSCs include thyristors with self-turn off capability (GTOs and IGCTs), silicon IGBTs and power MOSFETs. Because switching is performed irrespective of the grid frequency, higher switching frequencies can be used to reduce the size of passive components required for harmonic control and management. As a result SC-VSC stations are more compact thus making them ideal for off-shore wind energy conversion systems

- CS-LCCs are not capable of 4 quadrant operation and hence require reactive power compensation since the operation of the thyristor always causes current to lag voltage. In SC-VSCs, 4 quadrant operation is possible since there is complete control of the switching sequence.

The advantages of SC-VSCs listed above coupled with the emergence of off-shore wind energy conversion systems forced the technological migration of grid connected converters from thyristor based LCC systems to IGBT based VSC systems.

Developments in the manufacturing of high voltage IGBT power modules, with voltages ranging from 3.3 kV to 6.5 kV and current ratings up to 1.5 kA from Infineon, ABB and Mitsubishi [4-6], also promoted this technological migration since IGBTs started competing with thyristors in power handling capability. All the major power conversion companies from GE Power conversion (formerly ALSTOM grid) to ABB and Siemens have developed their variants of IGBT based VSC systems, with different nomenclatures and approaches [7]: HVDC Light from ABB [8], HVDC PLUS from Siemens [9] and ALSTOM HVDC MaxSine [10].

The first grid connected VSC system using silicon IGBTs was demonstrated in 1997 by ABB on a 3 MW ± 10 kV prototype with series connected IGBTs for off-state voltage sharing [8, 11, 12]. The first commercial link was installed in 1999, connecting the Swedish island of Gotland to the mainland. The rating of the VSC was 50 MW ± 50 kV [12].

The conventional packaging used for silicon IGBTs and the known reliability shortfalls discussed in previous chapters became a major concern. Failure in short circuit is critical in applications that use series connected IGBTs for sharing off-state voltage. Since IGBTs on DBC substrates do not guarantee failure in short, the development of

silicon IGBTs in pressure-packages became a requirement for grid connected VSCs. To this end, ABB developed the StakPak [13], which was simply IGBT devices in a pressure package assembly. Thyristors are typically 4 to 6 inch silicon wafers comprising of a 4-layer NPNP arrangement and conduct current via avalanche breakdown. IGBTs on the other hand are square or rectangular chips, which are incidentally also 4-layer, however, conduct current via drift-diffusion mechanisms in a MOS channel and a drift layer. Hence, a thyristor power module will comprise of a single wafer whereas an IGBT power module will be comprised of multiple chips connected in parallel for high current conduction capability.

There are two main architectures of press-pack IGBTs that have been commercialised. The first design comprises of the semiconductor chip sandwiched between two intermediate thermal contacts (for CTE matching) and conducting copper poles that also serve as heatsinks. Hence, unlike DBC systems, the cooling systems are not insulated. The pressure is applied globally from an external mechanical clamping system. This is the press-pack assembly design used by IXYS [14], which has also been used by Toshiba [15] and Fuji [16]. There is an insulating die carrier that aligns the semiconductor chip and intermediate thermal contacts. The die carrier also has an enclosure that insulates the conducting gate pin from the gate/collector power terminals. This design is hermetic and it uses an inert gas, namely SF₆ [17], for attenuating the electric fields within the module.

The main weakness in this design is the potential lack of uniformity in pressure that is applied across the different chips, as it is affected by dimensional tolerances of mechanical components and thermal deformation. As the power module degrades over time, there is potential loss of pressure uniformity as mechanical deformation occurs at the module edges. The second design is a more sophisticated approach taken by ABB that relies on each semiconductor chip supported mechanically by a dedicated individual spring that applies a mechanical force using the spring constant. In the ABB StakPak [13], the chips are soldered onto a molybdenum base plate with a fixture to keep the springs in place. The spring applies the force to an intermediate contact made of molybdenum or aluminium, depending on the mode of operation desired for the module and the kind of short-circuit failure desired [18]. Since each chip has a dedicated spring and the entire module is clamped externally, there is a self-compensation mechanism that ensures

pressure uniformity. Pressure uniformity in this design relies more on variability between the spring constant between the different springs than uniformity in the global clamping system. Hence, this is a more robust design. The StakPak is not hermetic and silicone gel is used for the mitigation of the electric fields within the module.

Both press-pack IGBT packaging alternatives are presented in Figure 5.3 and Figure 5.4. Figure 5.3 presents the ABB StakPak, where the individual springs for applying the force on each chip are clearly identified. Each sub-assembly of the StakPak is comprised of various chips, which can be IGBTs or diodes (for enabling reverse conduction). As it can be observed from Figure 5.3(a) and Figure 5.3(b), these sub-assemblies are fitted in a fiberglass reinforced frame, which allows different sizes and current ratings.

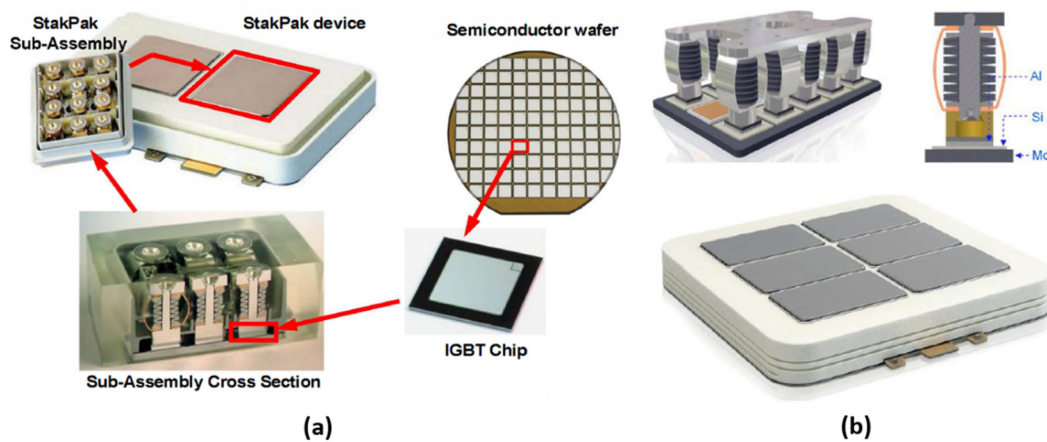


Figure 5.3 (a) StakPak packaging diagram. From chip to module [19] (b) StakPak submodule, detail of the individual spring connection and complete module [20]

The more conventional press-pack packaging approach, where a common force is applied to the module is shown in Figure 5.4. An individual die carrier is used for aligning the intermediate contacts and the chips, as well as for positioning the gate contact pin, as shown in Figure 5.4(b). The hermetic enclosure of the press-pack module is shown open in Figure 5.4(c).

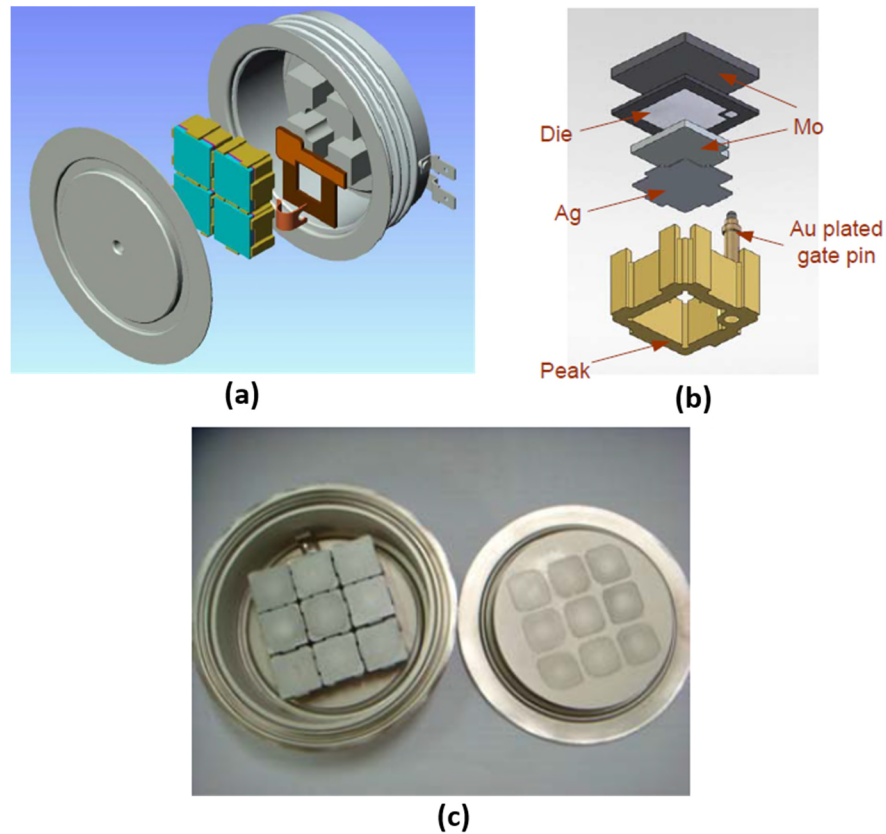


Figure 5.4 (a) 3D model explosion of a press-pack IGBT module from IXYS [21] (b) Exploded view of a 3D model of the die carrier assembly of the IXYS press-pack IGBT module [21] (c) Open IXYS press-pack IGBT capsule [21]

Press-pack IGBTs have found industrial implementation in grid connected voltage source converters and have been commercialised mainly by ABB and IXYS. Figure 5.5 shows the schematic diagram and picture of IXYS's press-pack IGBT power modules implemented in a 3 level neutral point clamped (3L-NPC) VSC which is available in 3.3 kV, 6.6 kV and 10 kV variants [22]. These converters can be used in on-shore wind energy conversion systems, distribution network FACTS and other power electronic based systems like medium voltage drives and marine drives [21, 23]. As an example, a study on a 3-level NPC converter for medium voltage drives converter using press-pack IGBTs is presented in [24], where the series connection of IGBTs for increasing the voltage rating is analysed.

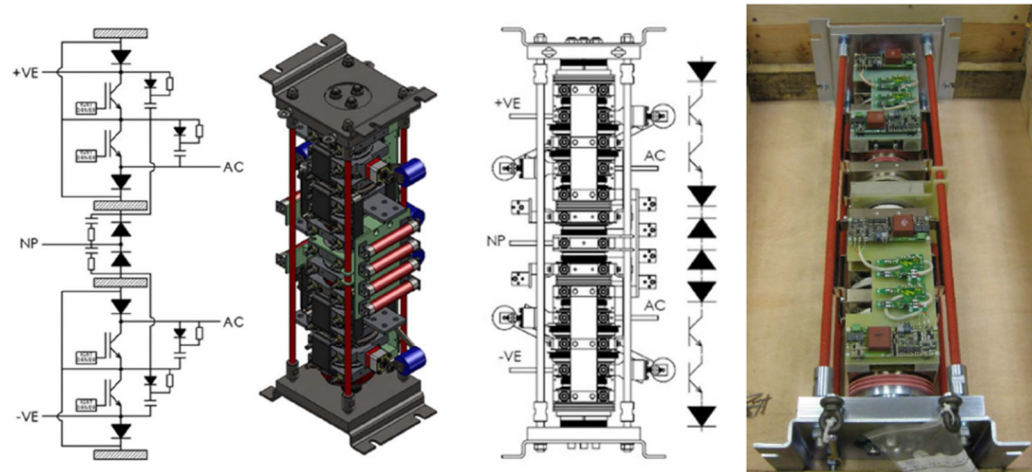


Figure 5.5 3.3 kV/1600 A Single phase stack of a 3-level NPC converter from IXYS [21]

SiC power devices are emerging as the main candidate for grid connected applications where power conversion efficiency and power density are key metrics. However, as stated in chapter 2, different research groups have shown that the different mechanical properties of SiC, including the higher Young's Modulus as well as the geometrical properties, potentially reduce the reliability performance under power cycling [25, 26]. As opposed to silicon devices, only few attempts of packaging of SiC devices using pressure contacts have been done [27, 28], however the enhanced surge current capability demonstrated in [29] and power cycling results in [30] suggest that it is a good packaging alternative for silicon carbide devices.

The integration of silicon carbide devices using pressure contacts follows the multichip approach used with silicon IGBTs, as defined previously. However, in the case of SiC chips, there is the added complexity of the smaller size of the silicon carbide chips compared with the contemporary silicon chip. This reduced chip size is a result of the manufacturing requirements to keep the defects at wafer level low [31] and it is enabled by the improved specific on-state resistance of silicon carbide devices. The demonstration and characterisation of SiC power devices in pressure packaging is a key technological challenge. As the voltage blocking capability of these devices increase, the electrothermal properties of SiC power devices in press-pack become more critical to characterise.

5.2 Design of a prototype for evaluation of pressure contacts in silicon carbide

A prototype for the evaluation of pressure contacts on SiC Schottky diodes has been designed. Figure 5.6 shows the prototype of a fully floating press-pack diode, including copper poles, intermediate contacts, the semiconductor chip and the external housing.

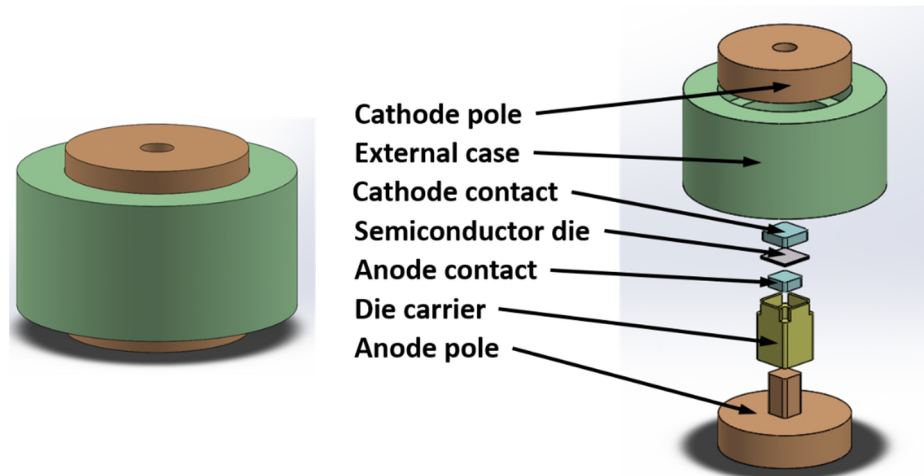


Figure 5.6 Prototype of a SiC Schottky diode using pressure contacts

This initial prototype is for a single diode chip and it has been designed for a 1200V/50A SiC Schottky diode model number CPW5-1200-Z050B from CREE/Wolfspeed. The size of the chip is 4.9 mm by 4.9 mm, with an anode opening of 3.8 mm by 3.8 mm and a thickness of 380 μm . Molybdenum is the traditional material for the intermediate contacts used in press-pack modules. Aluminium Graphite (ALG), a metal matrix composite by Schunk Hoffmann Carbon Technology [3], appears as a suitable alternative to molybdenum as intermediate contact for CTE matching. This alternative material will be studied in section 5.3.3., while the initial studies will be done using molybdenum as intermediate contact material.

The dimensions of the intermediate contacts are 3.7 mm by 3.7 mm for the anode contact and 4.9 mm by 4.9 mm for the cathode contact. Both contacts have a thickness of 1.5 mm and have been machined with a radius of 0.5 mm. The cathode contact made of molybdenum is shown in Figure 5.7.

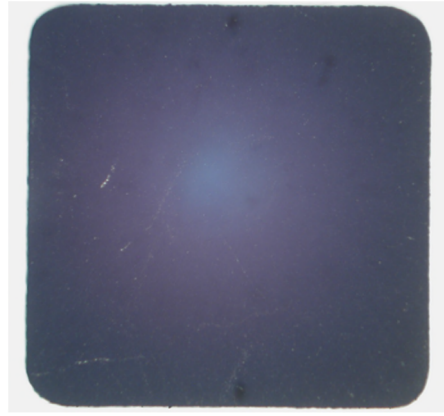


Figure 5.7 Picture of the cathode made of molybdenum

The pressed area is 13.48 mm^2 for the anode contact and 23.80 mm^2 for the cathode contact. A die carrier made of PPS is used for the alignment of the chip and the intermediate contacts while an external case made of PEEK is used for positioning the anode and cathode poles, made of copper with a $5 \text{ }\mu\text{m}$ nickel plating. A detailed cross-section of the prototype is shown in Figure 5.8, where the functionality of the die carrier can be observed.

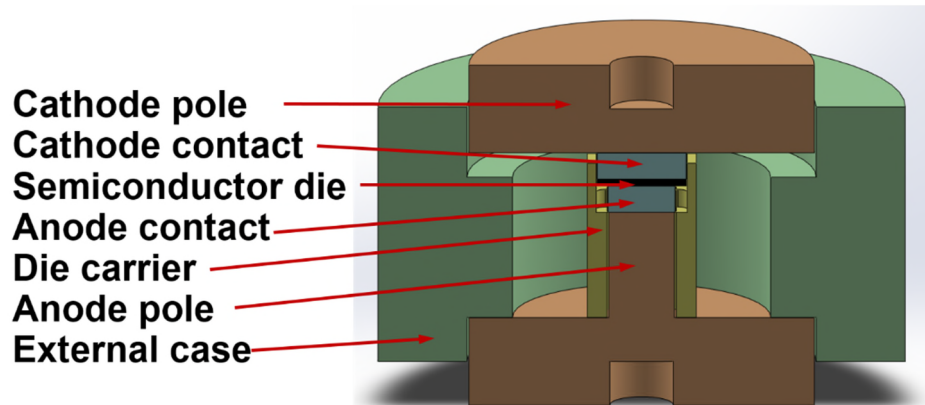


Figure 5.8 Cross-section of the press-pack diode prototype

The die carrier is a sensitive component of the system and it should comply the requirements for plastic materials used in power electronics modules, as described in [32]. Both PPS and PEEK are engineering plastics with a temperature of operation over 220°C , dimensionally stable, easy to machine and UL94/V0 compliant [33, 34]. Machinability is also a key requirement as the main function is to align the semiconductor chip and the intermediate contacts. A 3D model and a cross-section of the die carrier are

shown in Figure 5.9, while Figure 5.10 shows the die carrier assembled and how it used for aligning the semiconductor chip and the intermediate contacts.

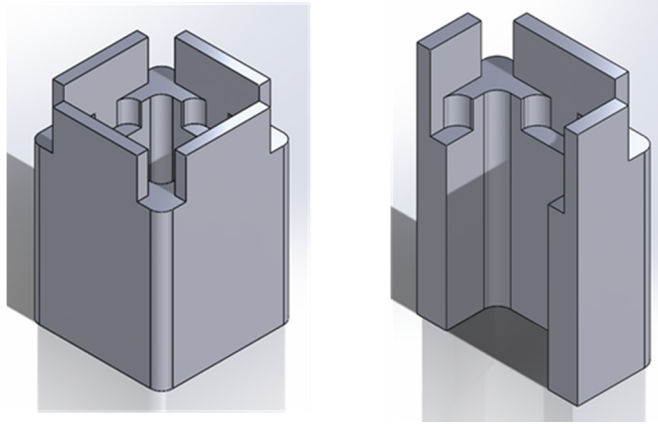


Figure 5.9 3D view of the die carrier prototype and cross-section

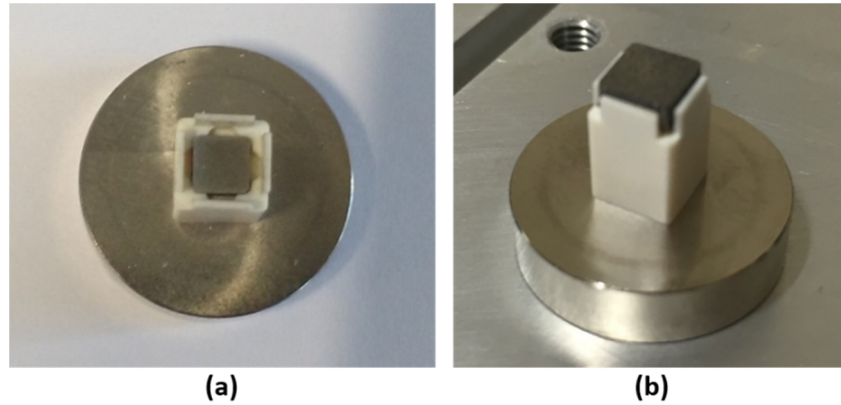


Figure 5.10 Details of the assembly of the prototype. (a) Anode contact and die carrier assembled, (b) Assembled prototype without the cathode pole and external case

The virtual prototype and pictures of a picture of a 200 A SiC Schottky diode in a pressure package are shown in Figure 5.11. The 200 A rated assembly, comprising four 50 A rated Sic Schottky diodes in parallel, will be evaluated in section 5.5.

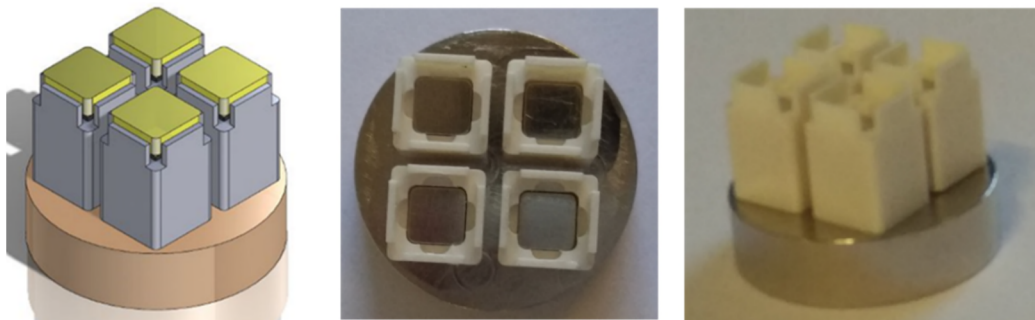


Figure 5.11 Details of a multiple chip press-pack SiC Schottky diode prototype

Table 5-I shows the component parts of the SiC press-pack diode prototype and the suppliers from which the parts have been retrieved.

Table 5-I Components used in the press-pack prototype

Parts	Supplier	Description
Clamp system	GD Rectifiers	Box clamp BX42, 300N, 500 N, 2000 N Clamp: BC79D, 400N Heatsinks: PS136/150B, PS260/150B, PS185/150B, Insulating standoffs
SiC Devices	CREE/Wolfspeed	Diode CPW5-1200-Z050B (1200 V, 50 A)
Contact Materials:	Schunk Hoffmann Carbon Technology	Anode and cathode intermediate contacts - ALG
	Saneway	Anode and cathode intermediate contacts - Molybdenum
Die Carriers	Fibracon/Roehling	Die carriers for chips and intermediate contacts External case of the module
Copper Electrodes	Abtech	Anode and cathode poles Copper – C101 - Nickel plating 5μ

5.3 Electrothermal characterisation

5.3.1 *Impact of the clamping force on the thermal resistance*

A pressure ranging from 10 N/mm² to 20 N/mm² is defined in [2] for optimal electrical and thermal contact hence, clamping forces ranging from 300 N to 500 N were selected for the studies presented in this thesis. The clamping force is applied using box clamps model BX42 from GD Rectifiers [35]. The assembly of the clamp with the module is shown in Figure 5.12(a). The clamp uses springs to apply the force on the module and is calibrated at a nominal clamping force for the height (19.38 mm) of the prototype. In order to achieve the best compensation possible, during the assembly of the module, the four bolts of the BX42 clamp are tightened sequentially, while the design of the clamp ensures that the force applied by the spring is orthogonal to the surface of the module. The principle of operation of the clamping mechanism is shown in Figure 5.12(b). It is important to note that this is a single side cooled assembly, hence the thermal resistance is higher than in a double side cooling system. However, the prototype presented is suitable for the evaluation of the impact of the clamping force on the electrical and thermal characteristics.

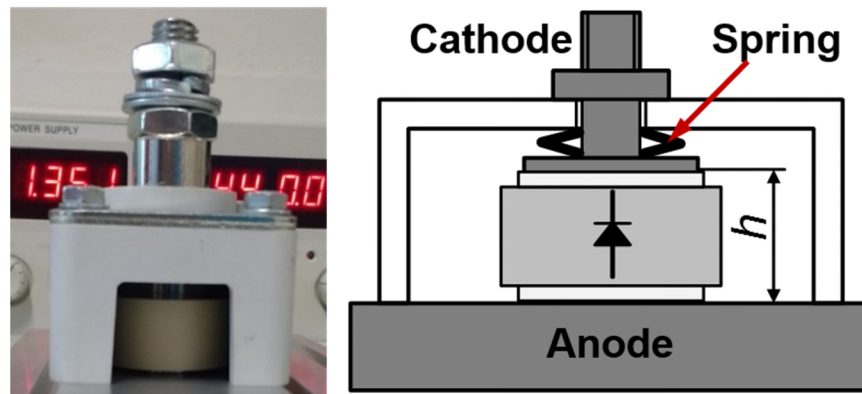


Figure 5.12 SiC Press-Pack Schottky diode with the clamping system used for electrical characterisation

The cumulative and differential structure functions of the press-pack prototype, as described in chapter 1, have been obtained for clamping forces of 300 N and 500 N, using special thermal characterisation equipment [36]. This characterisation has been done in the University of Nottingham. The cumulative structure function is shown in Figure 5.13 while the differential structure function is shown in Figure 5.14. The impact

of the clamping force on the thermal resistance is clearly observed with the thermal resistance for the 300 N force measured as $R_{TH-300N} = 2.31 \text{ }^{\circ}\text{C/W}$ while that of the 500 N force measured as $R_{TH-500N} = 2.16 \text{ }^{\circ}\text{C/W}$.

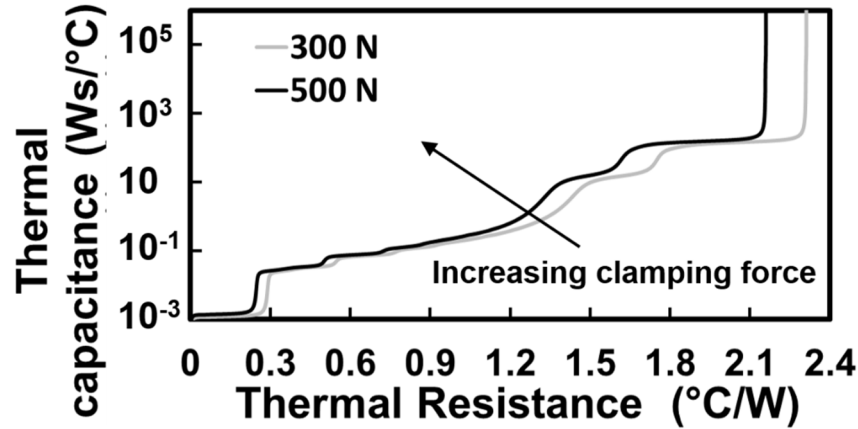


Figure 5.13 Impact of the clamping force on the cumulative structure function for the press-pack diode

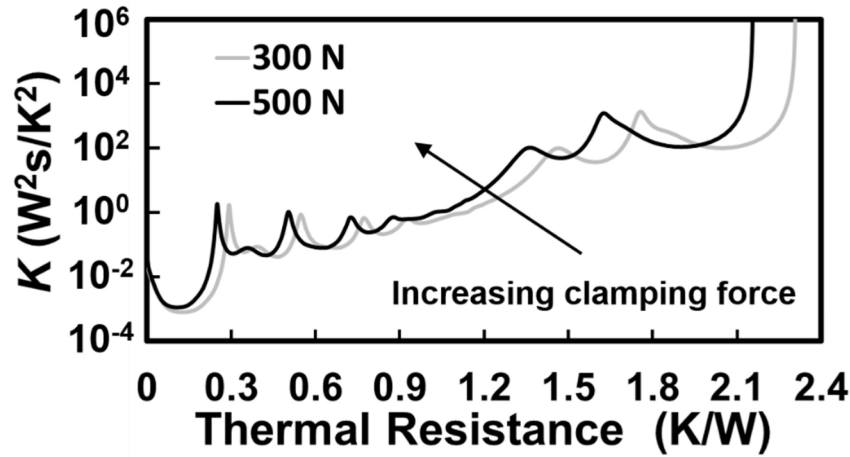


Figure 5.14 Impact of the clamping force on the differential structure function for the press-pack diode

The thermal resistances and capacitances are determined by the material properties, but when pressure contacts are used, a contact resistance is added to the static thermal network, as it is shown in Figure 5.15 [37], where the contact resistances ($R_{th,material-material}$) and thermal resistances ($R_{th,(material)}$) are identified for the different elements of the press-pack module. The contact resistance is a function of the clamping force and it is also affected by properties like the flatness, roughness, metallization of the

elements in contact and hardness [30, 38]. For a transient thermal impedance analysis the thermal capacitances are added to the thermal network.

Figure 5.15 shows a double side cooled assembly of the proposed prototype. In this case both anode and cathode poles are connected to a heatsink, hence the case temperature (T_C) on both sides is assumed to be equal, opposed to the single side cooling assembly. The junction temperature (T_J) is defined as the temperature at the centre of the die.

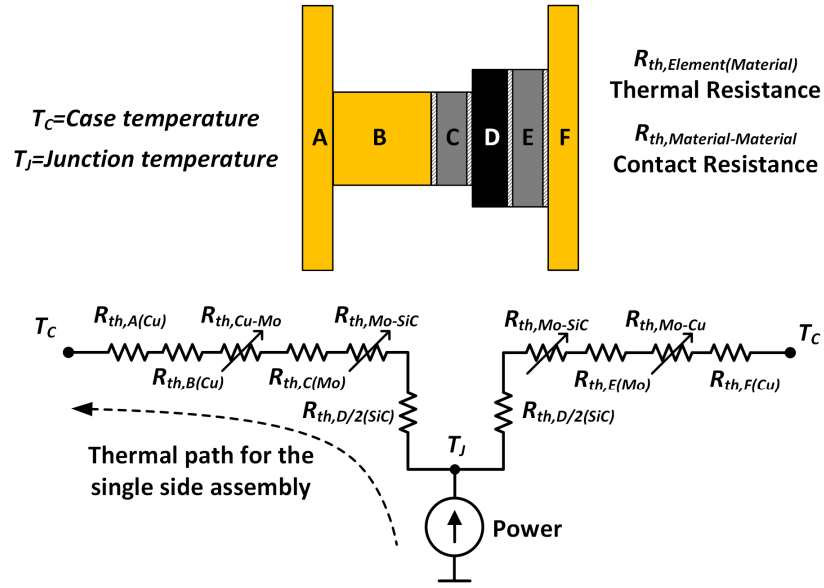


Figure 5.15 Static thermal network of the press-pack diode for double side cooling, where the thermal path for single side cooling is identified

The characterisation of the press-pack module presented previously in Figure 5.13 and Figure 5.14 was performed using a single side cooling system, where the anode pole was connected to the heatsink, as shown in Figure 5.12. For this single side assembly, the direction of heat flow, as shown in Figure 5.15 is from the power semiconductor chip (label D) through the intermediate contact (label C), through to the anode pole which comprises of a protruding section (labelled B) and the base (labelled A) which is connected to the heatsink. Equation (5.1) can be used for determining the thermal resistance of each element, where d is the thickness of the material, A the cross-section and λ the thermal conductivity.

$$R_{TH,material} = \frac{d}{\lambda A} \quad (5.1)$$

Analysing equation (5.1), the thermal resistance is inversely proportional to the cross-sectional area of the material and directly proportional to the length of the thermal path. Hence, it is clearly observed that the thermal path (from D to A) of the single side cooled prototype, coupled with additional contact resistances, will yield a higher thermal resistance compared to traditional solder based systems. However, using a double side cooling system, which is one of the main benefits of the press-pack assembly, will minimise the impact of the pedestal on the thermal performance as it will be demonstrated later in this chapter. Here, with respect to Figure 5.15, the heat will flow from the device (D) to both poles (A and F). Hence, the single side cooled prototype presented here, has not been designed for an optimal thermal performance, nevertheless, it is suitable for the evaluation of the impact of the clamping force on the electrical and thermal characteristics as well as an assessment of its reliability.

5.3.2 Impact of the clamping force on the electrical resistance

Referring back to Figure 5.13, the thermal resistance for a clamping force of 300 N force is $R_{TH-300N} = 2.31 \text{ K/W}$ while for a clamping force of 500 N, the measured value is $R_{TH-500N} = 2.16 \text{ K/W}$, indicating a global reduction of thermal resistance of 0.15 K/W. Increasing the clamping force has also an impact on the electrical contact resistance and this has been evaluated in this thesis.

The impact of the electrical contact resistance on the forward voltage has been evaluated using the experimental set-up represented by the schematic diagram shown in Figure 5.16 and Figure 5.17, where the box clamp was attached to a heatsink model PS136/150B from GD Rectifiers [35]. In this set-up, the heating current is passed through the diode to raise the junction temperature through the self-heating of the device.

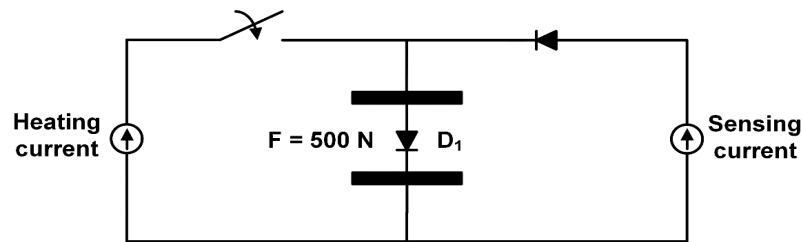


Figure 5.16 Electrical schematic of the electrothermal characterisation test set-up

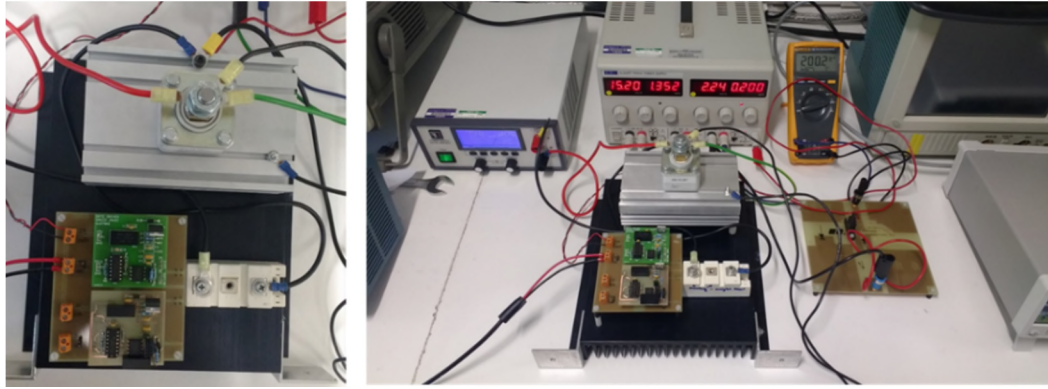


Figure 5.17 Experimental test set-up for the SiC Schottky diodes in Press-Pack

The different thermal resistances and forward voltages that result from the different clamping forces cause different junction temperatures on the chip. A low sensing current can be used to measure the junction temperature through the forward voltage, as TSEP defined in chapter 2, and an auxiliary diode is used for isolating both power supplies. This is done after the heating current is switched off and the sensing current is used to measure the forward voltage during the cooling phase of the device.

As it was defined in chapter 2, the temperature dependency of the forward voltage must first be determined so that a look-up-table or a calibration table can be created and used to translate measured forward voltages into junction temperatures. This calibration table was developed by measuring the forward voltage at different temperatures after the junction temperature of the device was set by a thermal chamber. By allowing enough time to reach steady state, the temperature of the chamber can be considered equal to the junction temperature. Using a low value sensing current of I_{SENSE} to minimise the self-heating, the forward voltage was measured at different temperatures for clamping forces of 300 N and 500 N. The calibration curves are shown in Figure 5.18, for different clamping forces and sensing currents of 100 mA and 200 mA.

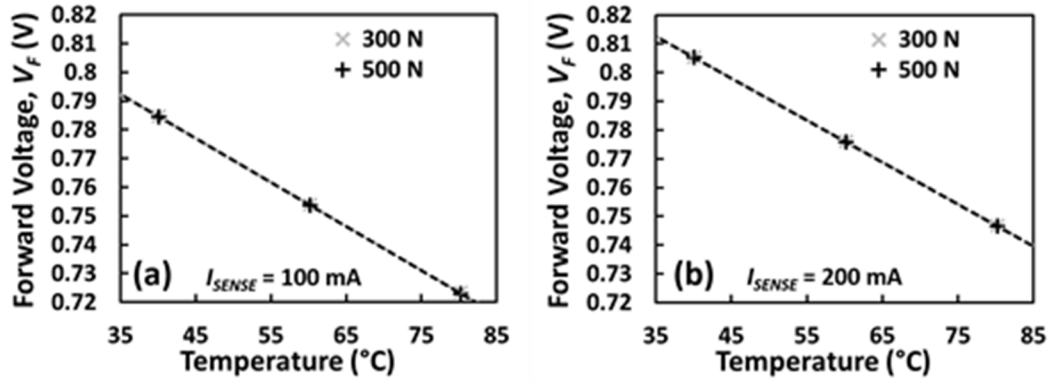


Figure 5.18 Calibration of the forward voltage as TSEP for molybdenum contacts.
(a) Sensing current 100 mA (b) Sensing current 200 mA

Different magnitudes of DC heating currents, each 15 seconds long, were used for evaluating the electrical and thermal characteristics of a single diode module with pressure contacts applied by 300 N and 500 N clamps. The results for the forward voltage are presented in Figure 5.19 for both 300 N and 500 N forces, where heating currents ranging from 6 A to 30 A were used.

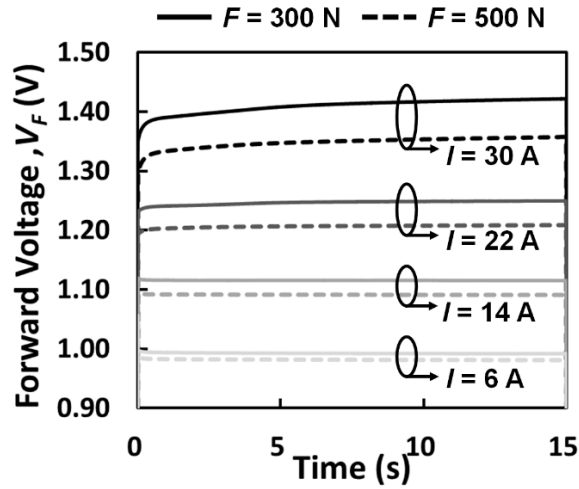


Figure 5.19 Impact of the clamping force on the forward voltage for different currents

From the results presented in Figure 5.19 it can be observed that for a reduced clamping force, the forward voltage of the diode for the same current is higher, hence leading to higher power losses in the diode. This is expected since the electrical contact resistance is inversely proportional to the clamping force and the forward voltage is proportional to the contact resistance.

Using the measured forward voltage across the prototype the impact of the clamping force can be evaluated. Using the simplified schematic shown in Figure 5.20, where the electrical contact resistances ($R_{material-material}$) and electrical resistances ($R_{(material)}$) are identified for the different elements of the press-pack module, the forward voltage across the module for a current I , $V_{F,I}$, is given by equation (5.2). In equation (5.2), $V_{AK,I}$ is the forward voltage across the chip for a current I while $\Sigma R_{X(Material)}$ and ΣR_{X-Y} are the sum of the electrical and contact resistances respectively.

$$V_{F,I} = V_{AK,I} + I \cdot \left(\sum R_{X(Material)} + \sum R_{X-Y} \right) \quad (5.2)$$

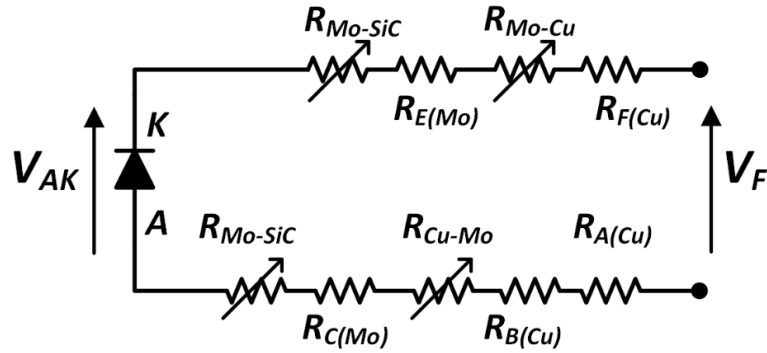


Figure 5.20 Electrical schematic of the press-pack diode

The only term in equation (5.2) directly dependent of the clamping force is the contact resistance R_{X-Y} . Hence, assuming temperature invariance for short current pulses, the internal diode forward voltage and the voltage drop across the contacts can be assumed constant. The measured voltage across the press-pack assembly, including the clamp and heatsink, for a series of currents ranging from 10 to 30 A, at 300 N and 500 N clamping forces, is presented in Table 5-II. The relationship between the contact resistances at two different forces can be written as (5) which was used for calculating the difference in contact resistance caused by the different clamping force.

$$V_{F1,I} - V_{F2,I} = I \cdot (\Sigma_{F1} R_{X-Y} - \Sigma_{F2} R_{X-Y}) \quad (5.3)$$

The forward voltage was measured after 20 ms, using the data from Figure 5.19. From the presented results, the average contact resistance reduction from using a clamping force of 500 N instead of 300 N is 1.748 m Ω

Table 5-II Impact of the clamping force on the forward voltage and contact resistance. Molybdenum contacts and assembly with small heatsink

Current (20 ms pulse)(A)	$V_{300N,I}$ (V)	$V_{500N,I}$ (V)	$\Sigma R_{X-Y} - \Sigma R_{X-Y}$ (mΩ)
10	1.0597	1.0423	1.741
14	1.1185	1.0944	1.723
18	1.1756	1.1445	1.702
22	1.2320	1.1953	1.669
26	1.2956	1.2470	1.867
30	1.3541	1.3005	1.786

The different thermal resistance determined by the clamping force will have an impact on the junction temperature and, as it was mentioned previously, it can be estimated using the calibrated TSEP. The junction temperature increase for the different DC heating pulses is presented in Figure 5.21, where the junction temperature rise is shown as a function of the DC heating current magnitude. It can be seen that the temperature rise reduces with the increased clamping force. Hence, it is important in pressure contact power modules that the clamping force remains as constant and homogeneous among the different chips as possible over the mission profile of the application. Loss of contact force will increase the thermal resistance and junction temperature.

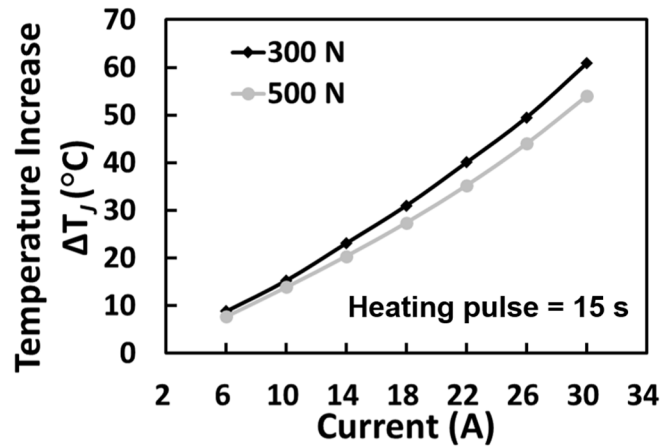


Figure 5.21 Impact of the clamping force on the junction temperature increase for different heating pulses

5.3.3 Impact of the intermediate contact material on the contact resistances

ALG is a Metal Matrix Composite (MMC) produced by pressure infiltration of porous graphite by liquid aluminium. According to Schunk Hoffmann [3], this new composite incorporates the advantageous properties of both materials and can be used as an alternative to molybdenum in press-pack modules because of its suitable CTE and thermal conductivity. The type of ALG used in this study is ALG 2208, which is an anisotropic material, and its properties, compared with Molybdenum and silicon carbide are shown in Table 5-III. With a suitable CTE and a high thermal conductivity, as it is shown in Figure 5.22, the electrothermal performance in press-pack assemblies of this alternative material will be evaluated in this section of the thesis.

Table 5-III Properties of ALG2208, Molybdenum and SiC [25, 39]

	ALG2208	Molybdenum	SiC
Thermal Conductivity ($\mu\text{m}/\text{m}^\circ\text{C}$)	x,y: 220 z: 140	138	380
Thermal Capacity ($\mu\text{m}/\text{m}^\circ\text{C}$)	800	217	690
Density (kg/m^3)	2300	10220	3210
CTE ($\mu\text{m}/\text{m}^\circ\text{C}$)	x,y: 8 z: 12	5.35	4.3
Resistivity (Ω/m)	x,y: 4e^{-7} z: 6e^{-7}	5.3e^{-8}	-

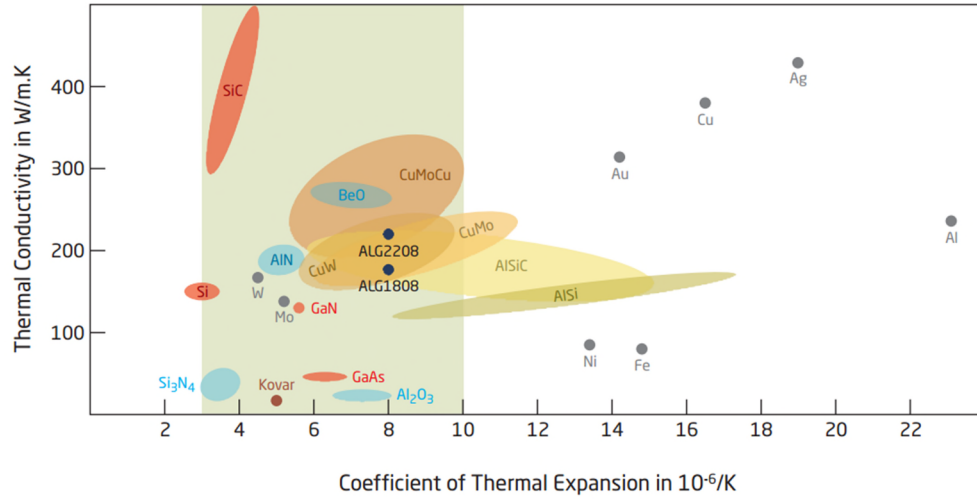


Figure 5.22 Comparison of the thermal conductivity and the coefficient of thermal expansion of ALG with different materials used in power module packaging, from [40]

Figure 5.23 presents different pictures of the ALG contact, where the aluminium and graphite structure is easily identified.

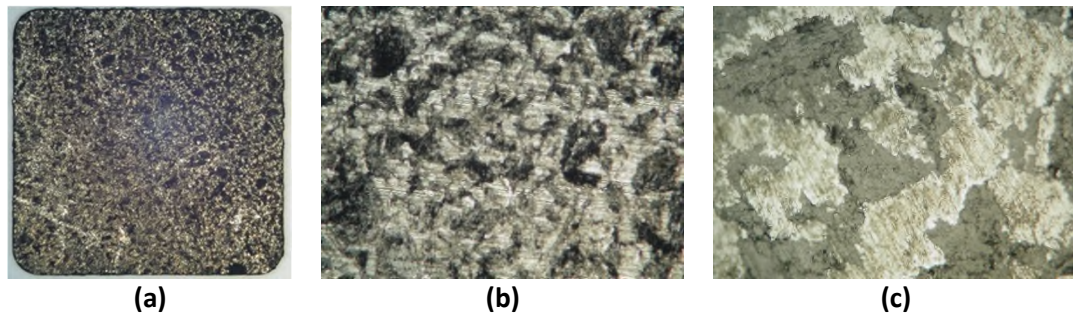


Figure 5.23 Details of the ALG contact. 2x, 10x, 50x

As it was mentioned before, the roughness and flatness of the surfaces in contact would have an impact on the electrical and thermal contact resistances. For this study the contacts have not been plated, hence the surface characterisation of the non-plated molybdenum and ALG contacts was performed. The surface of the contacts was characterised using a ContourGT-X 3D Optical Microscope from Bruker [41]. These characterisations are shown in Figure 5.24. The average surface roughness S_A is $0.763 \mu\text{m}$ for the molybdenum contacts and $0.736 \mu\text{m}$ for the ALG contacts. Despite having a similar average surface roughness, in Figure 5.24(b) the effect of the different materials composing the ALG structure can be observed. A 3D view of the characterisation of the ALG contact is shown in Figure 5.25.

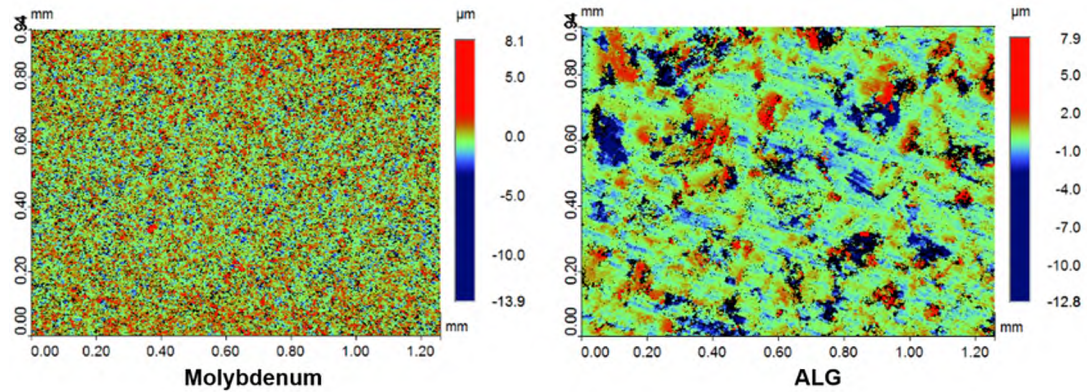


Figure 5.24 Surface characterisation of the molybdenum and ALG contacts

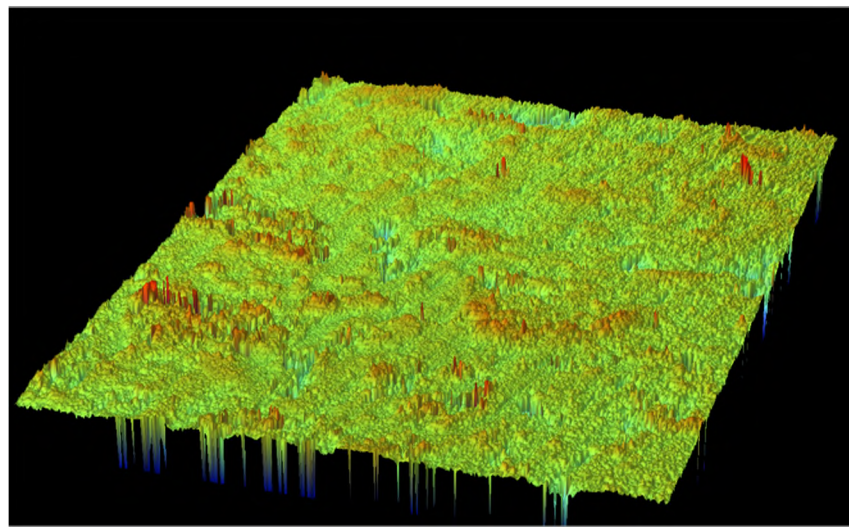


Figure 5.25 Three-dimensional surface characterisation of the ALG contact

Using the same thermal characterisation equipment [36] which was used for the characterisation of the differential and cumulative structure function of the press-pack diode using molybdenum contacts in section 5.3.1, the structure functions of the prototype using ALG contacts were obtained. These structure functions were obtained at the University of Nottingham, where the equipment is available.

Figure 5.26 presents the cumulative structure function for clamping forces of 300 N and 500 N, where a reduction of the thermal resistance as the clamping force increases is clearly identified. The thermal resistance for a clamping force of 300 N is 1.95 K/W while the thermal resistance for a clamping force of 500 N is 1.82 K/W indicating a reduction of the global thermal resistance of 0.13 K/W. The differential structure function for the ALG assembly is shown in Figure 5.27.

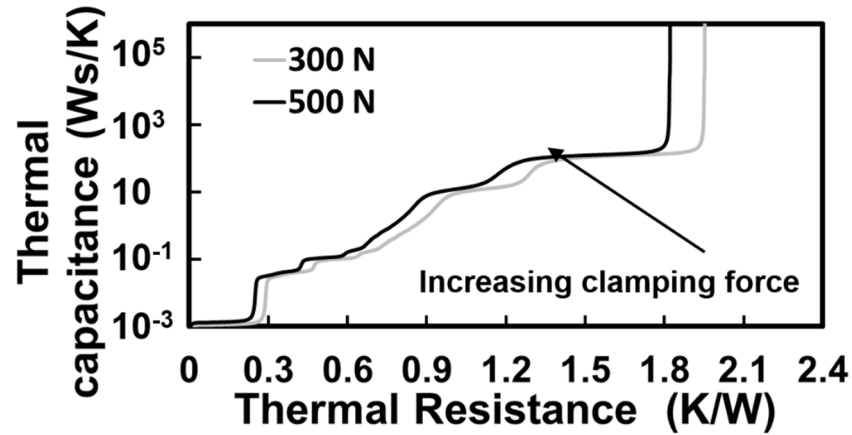


Figure 5.26 Cumulative structure function for difference clamping forces. ALG as intermediate contact.

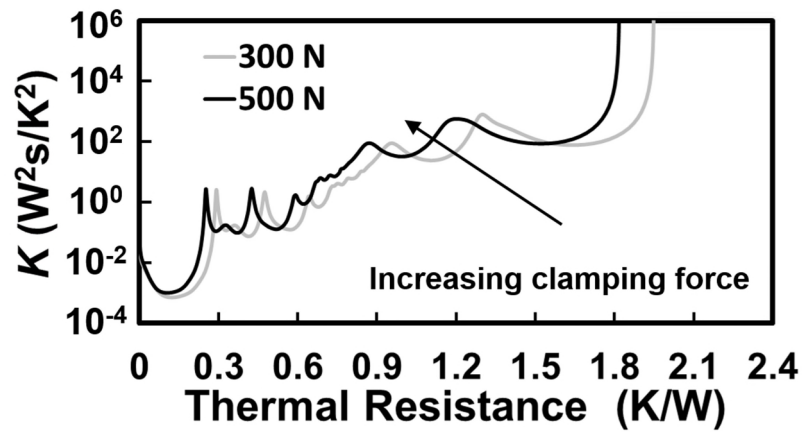


Figure 5.27 Differential structure function for difference clamping forces. ALG as intermediate contact.

The comparison of the thermal resistances of the prototype using ALG and molybdenum intermediate contacts can be done using the structure functions obtained for both contacts. Figure 5.28 presents the differential structure function for both ALG and molybdenum contacts and a clamping force of 300 N while Figure 5.29 presents the differential structures for a clamping force of 500 N.

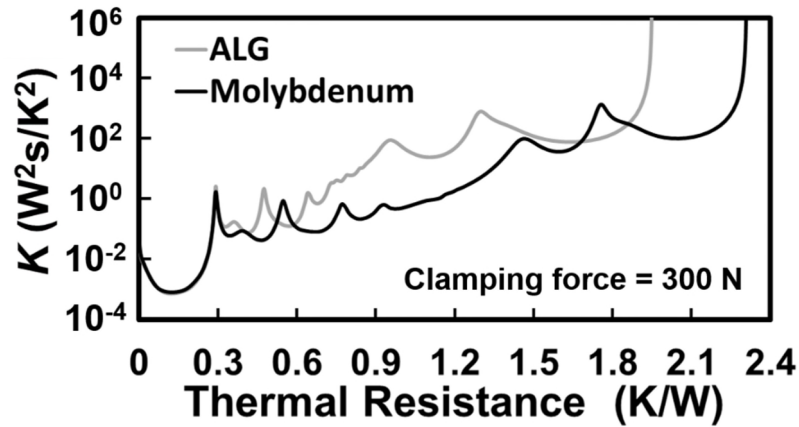


Figure 5.28 Comparison of the differential structure function for ALG and Molybdenum for a clamping force of 300 N

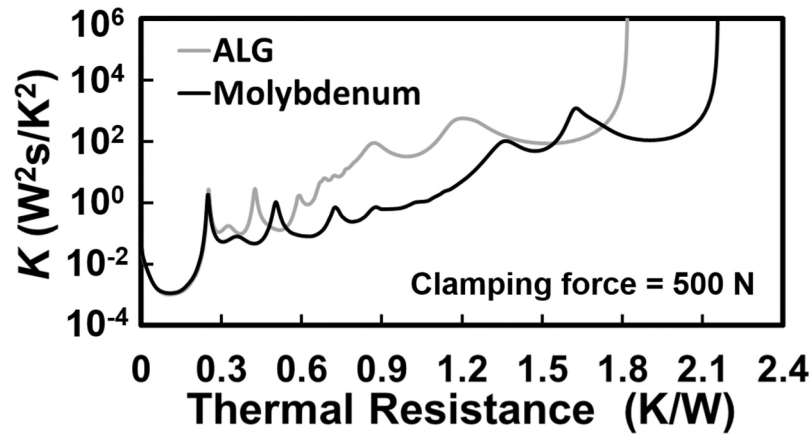


Figure 5.29 Comparison of the differential structure function for ALG and Molybdenum for a clamping force of 500 N

In both Figure 5.28 and Figure 5.29 it can be observed that there is a region coincident for both clamping materials and there is also a peak, which in the case of the differential structure function represents a change of material in the heat path. Assuming that the semiconductor chip is the same for both contact materials and that the thermal resistance is calculated from the source of the heat to the heatsink, that section can be identified as the chip. Evaluating both contact materials together, it can be easily observed from Figure 5.28 how for a clamping force of 300 N the use of ALG of intermediate contact material improves the thermal resistance of the prototype in 0.36 K/W, indicating a reduction of approximately 15.6 % on the thermal resistance.

The impact of the clamping force on the electrical resistance when ALG contacts are used can be done using the forward voltage, as it was done for the molybdenum contacts in section 5.3.2. The forward voltage for the assembly using ALG contacts was characterised at different DC currents, for clamping forces of 300 N and 500 N. The press-pack assembly used for this characterisation composed of a box clamp BX42 rated at the evaluated force and a heatsink model PS260/150B, both from GD Rectifiers. The electrical schematic is the same than the electrical schematic shown in Figure 5.16 and Figure 5.17, but replacing the heatsink model PS136/150B with a heatsink model PS260/150B.

In order to establish a fair comparison between the use of ALG contacts and molybdenum contacts, the forward voltage for molybdenum contacts was characterised again using this new press-pack assembly. The forward voltage, captured during self-heating of the diode at different current levels is shown in Figure 5.30 for the ALG and molybdenum intermediate contact. For both contact materials, evaluating Figure 5.30(a) and Figure 5.30(b) it can be observed that increasing the clamping force reduces the on-state voltage, hence indicating a reduction of the contact resistance for both molybdenum and ALG contacts. This was expected from the results presented in section 5.3.2. Comparing both voltages, the on-state voltage is higher when ALG contacts are used.

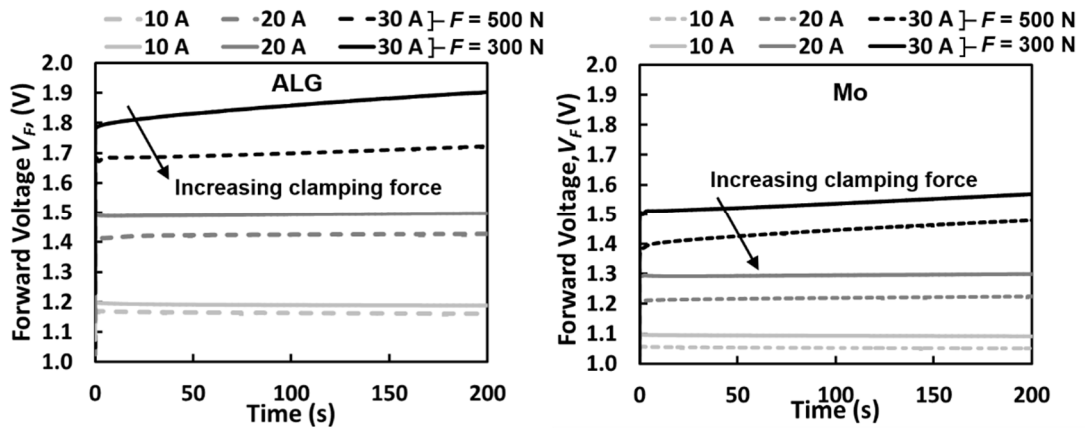


Figure 5.30 Impact of the clamping force on the forward voltage during self-heating (a) ALG contacts (b) Mo contacts

Using the same procedure which was described in section 5.3.2, the impact of the clamping force on the global contact resistance has been calculated for ALG and molybdenum contacts using the on-state voltage after 20 ms, in order to consider the

impact of the self-heating on the electrical resistances negligible. The average contact resistance reduction from using a clamping force of 500 N instead of 300 N is 3.640 m Ω for ALG intermediate contacts, while the average contact resistance reduction for molybdenum contacts is 3.896 m Ω . The measured forward voltages and calculated difference in contact resistance are shown in Table 5-IV and Table 5-V for the ALG intermediate contacts and molybdenum intermediate contacts respectively.

Table 5-IV Impact of the clamping force on the forward voltage and contact resistance. ALG contacts and assembly with large heatsink

Current (20 ms pulse)(A)	$V_{300N,I}$ (V)	$V_{500N,I}$ (V)	$\Sigma R_{X-Y} - \Sigma R_{X-Y}$ (mΩ)
10	1.197	1.167	2.932
20	1.480	1.400	4.009
30	1.740	1.621	3.979

Table 5-V Impact of the clamping force on the forward voltage and contact resistance. Molybdenum contacts and assembly with large heatsink

Current (20 ms pulse)(A)	$V_{300N,I}$ (V)	$V_{500N,I}$ (V)	$\Sigma R_{X-Y} - \Sigma R_{X-Y}$ (mΩ)
10	1.1000	1.0583	4.175
20	1.2797	1.1960	4.182
30	1.4257	1.3258	3.331

The forward voltage has been characterised for molybdenum contacts in two different set of measurements, using different chips and heatsink assemblies, hence the different reduction of the global contact resistance between both sets of measurements. As it was mentioned in section 5.1, this design can be affected by the dimensional tolerances of the mechanical components and given the reduced force that is used for a single SiC chip because of the small chip size, these can result in differences in the electrical and thermal characteristics.

The measured forward voltages, after 20 ms of the heating pulse, for both tests at the same clamping force and molybdenum as intermediate contact material are shown in

Figure 5.31. Evaluating the results presented in Figure 5.31(b), it is clearly observed how for a clamping force of 500 N the results are similar, with a variation of the forward voltage around 1.7 %, which can be attributed to dimensional tolerances or differences in the contacts. However, in the case of the clamping force of 300 N, as the results in Figure 5.31(b) show, the difference between both calibration measurements is clearly observed, with an average variation of 4.5 %. This can be caused by a lower clamping force resulting from dimensional tolerances of the mechanical elements of the clamp, a different Hook's constant for the spring which applies the clamping force or a clamp not adjusted properly, hence resulting in a force lower than the nominal. This variation of clamping force will have an impact in the case of multiple chip modules, leading to an uneven clamping force between chips, and it is evaluated in section 5.5 of this chapter.

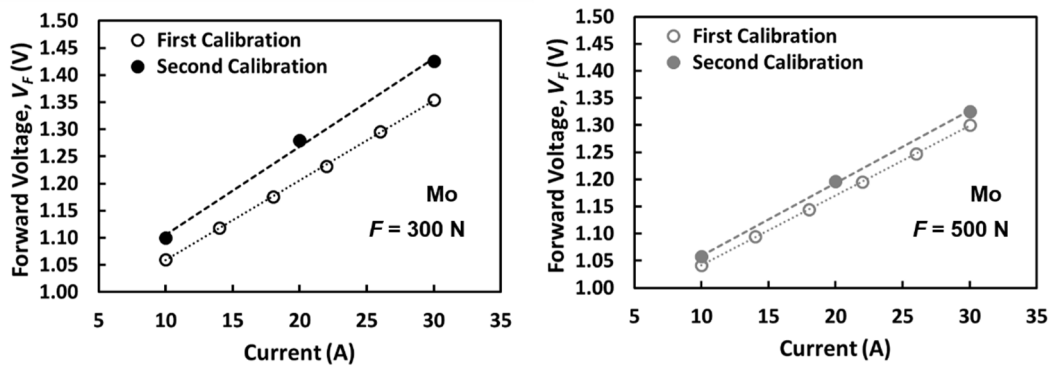


Figure 5.31 Measured forward voltage after 20 ms for molybdenum contacts and different clamping forces during two different calibration measurements. (a) $F = 300$ N, (b) $F = 500$ N

As it was done with the molybdenum contacts, the temperature dependency of the forward voltage at low currents for the press-pack diode using ALG contacts should to be calibrated, in order to be able to use the forward voltage as TSEP. This calibration has been done using a thermal chamber, following the same procedure that was used for the molybdenum contacts, described in section 5.3.2. The calibration curves for ALG contacts, at different clamping forces and sensing currents are presented in Figure 5.32.

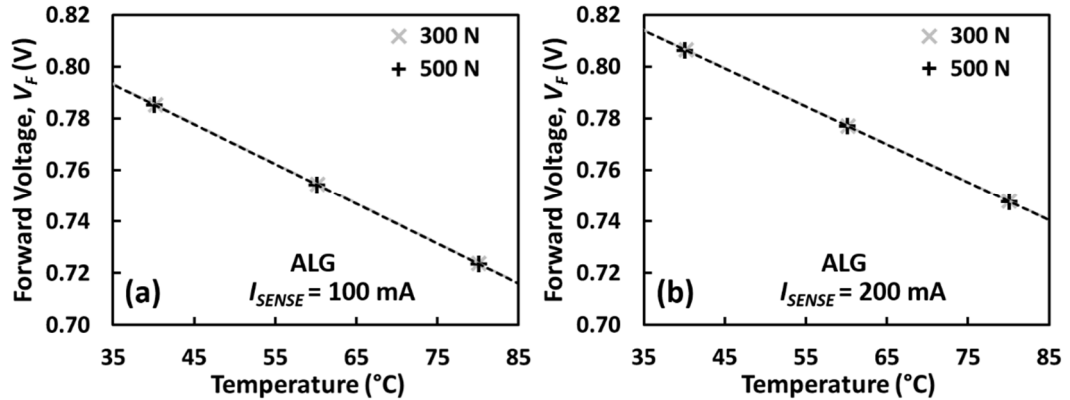


Figure 5.32 Calibration of the forward voltage as TSEP for molybdenum contacts and different forces (a) Sensing current $I_{SENSE} = 100$ mA, (b) Sensing current $I_{SENSE} = 200$ mA

Referring back to Figure 5.18, which shows the calibration of the forward voltage when molybdenum contacts are used, and comparing with Figure 5.32, which presents the calibration for ALG contacts, the use of both materials results in a similar temperature coefficient, or K- factor. The temperature coefficient is calculated as the slope of the trend line and it is around -1.5 mV/°C for the different contacts and clamping forces. As the results in Figure 5.18 and Figure 5.32 indicate the clamping force has a minor impact on the calibration curve. However, as it was identified during the DC heating tests at high currents done with the press-pack Schottky diode presented previously, the higher resistivity of the ALG contacts has also an impact when both calibration curves are compared. The calibration curves for both ALG and molybdenum contacts for a clamping force of 500 N and a sensing current of 200 mA are shown in Figure 5.33, where it is observed that the forward voltage is slightly higher when ALG contacts are used.

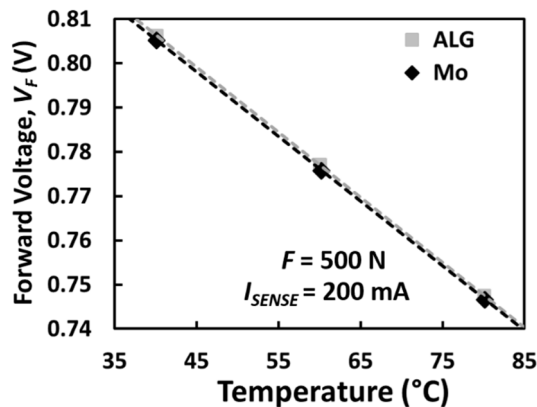


Figure 5.33 Calibration of the forward voltage as TSEP for molybdenum contacts and ALG contacts

5.3.4 Transient heating tests

Heating tests were performed at different clamping forces for the two contact materials and different load currents using the test circuit shown in Figure 5.16. A small heatsink, model PS136/150 and a large heatsink model PS185/150B, both from GD rectifiers were used for this tests. Both heatsink assemblies use the box clamp BX42, as it is shown in Figure 5.34. It is important to remark that for these assemblies insulating standoffs are required as the heatsinks are live.

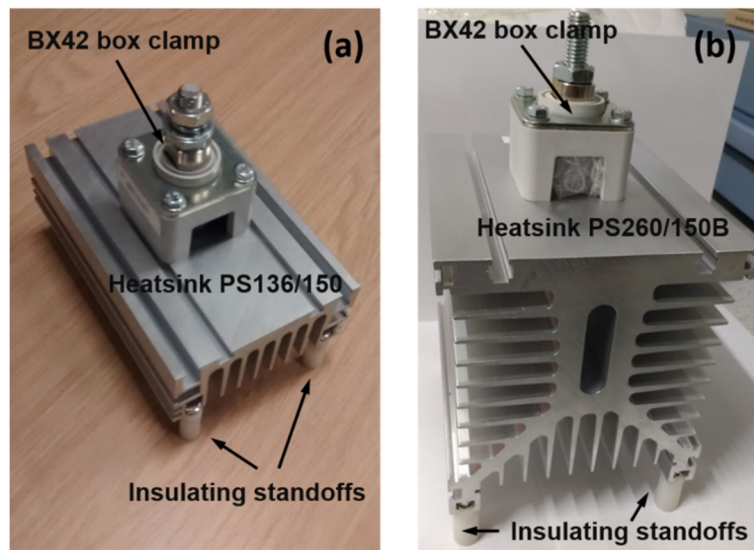


Figure 5.34 Single side heatsinks used for evaluation of the thermal response of the intermediate contacts. (a) Heatsink Model PS136/150 (b) Heatsink model PS260/150B

The impact of the contact material has been evaluated using assemblies with the large heatsink (model PS260/150B) and a box clamp rated at 500 N. The press-pack assembly, namely the clamp, device and heatsink, was used as part of the test setup shown in Figure 5.17. Heating pulses of different current levels and duration were used to increase the temperature of the chip, using both ALG and molybdenum intermediate contacts. Once the heating current was switched off, the calibrated TSEP, for the respective clamping force and contact material was used for estimating the junction temperature and the junction temperature increase ΔT_j caused by the heating pulse.

The results are presented in Figure 5.35 and it is clearly observed that the use of ALG contacts improves the thermal performance of the press-pack diode, as the lower thermal resistance measured using the thermal characterisation equipment indicated. It is

important to indicate that this tests have been performed using constant current, hence the power dissipated when ALG contacts are used will be higher, given the higher on-state voltage compared with the molybdenum assembly.

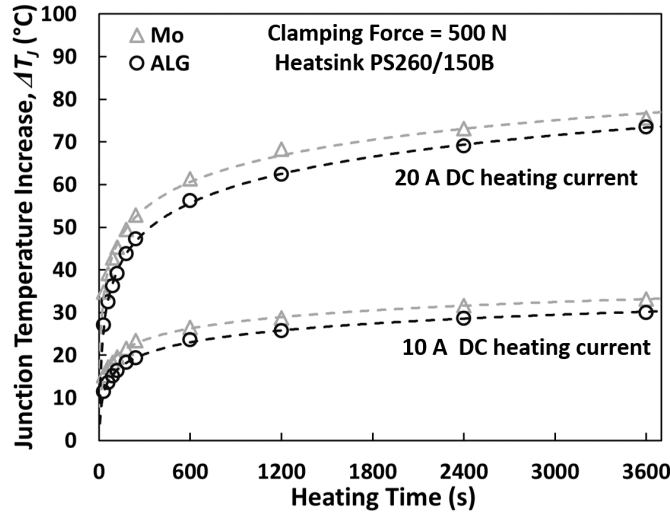


Figure 5.35 Transient heating of the assembly using the large heatsink. ALG and molybdenum contacts, clamping force 500 N

The impact of the clamping force on the thermal performance has been evaluated using ALG as intermediate contact. Tests were performed using the small heatsink and the large heatsink assemblies and the results are presented in Figure 5.36. It is clearly observed how increasing the clamping force reduces the junction temperature increase, hence verifying the improvement of the thermal resistance. Using the large heatsink, with a lower thermal resistance, also reduces the junction temperature increase for the same clamping force.

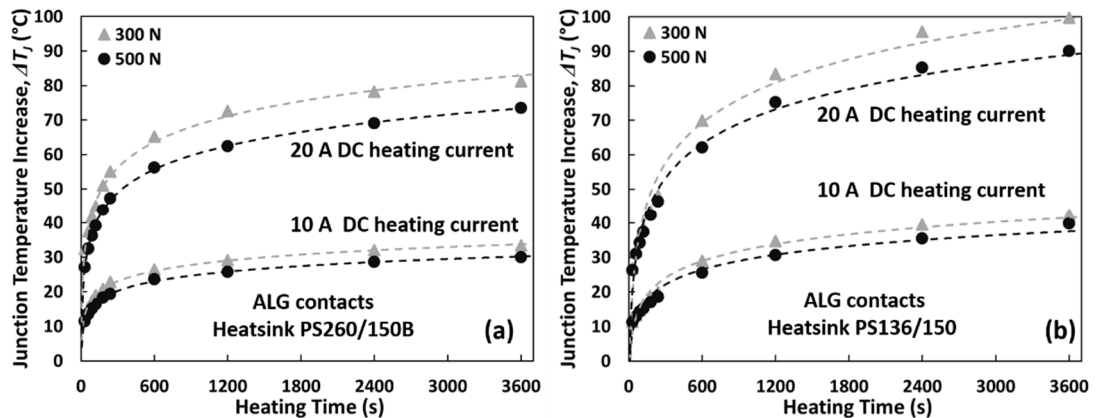


Figure 5.36 Impact of the clamping force on the transient heating using ALG contacts. (a) Large heatsink assembly (b) Small heatsink assembly

Similar results have been obtained for the intermediate contact made of molybdenum, with the impact of the force on the transient thermal response for the large heatsink presented in Figure 5.37.

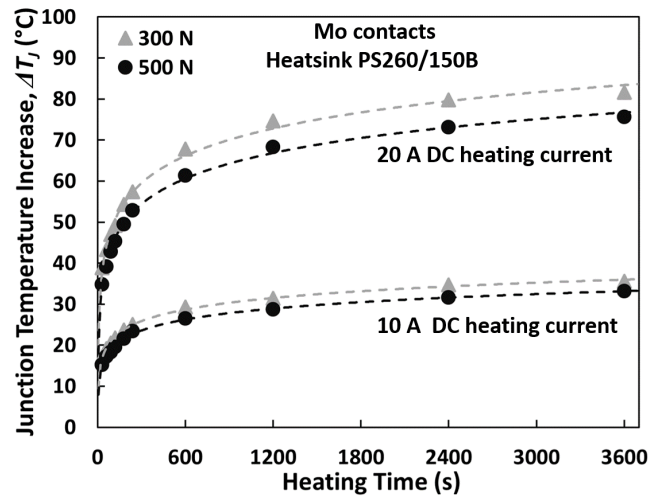


Figure 5.37 Impact of the clamping force on the transient heating of the assembly using molybdenum contacts and the large heatsink assembly

The results presented previously show that both increasing the clamping force or the size of the heatsink reduce the junction temperature, however one of the main benefits of the press-pack packaging system is that it allows to use double side cooling. In order to verify that, a double side cooled assembly has been prepared and tested. Two heatsinks model PS185/150B and a clamp model BC79D rated at 400 N for the nominal length of the prototype, both from GD rectifiers, have been used and the assembly is shown in Figure 5.38.

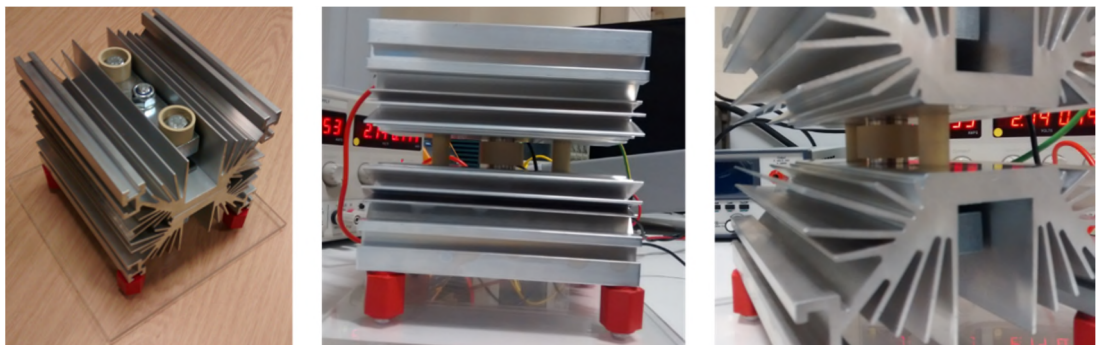


Figure 5.38 Pictures of the double side assembly of the press-pack diode prototype

The double side cooling system will minimise the impact of the pedestal on the anode copper pole and it will reduce the thermal resistance, hence a reduction on the junction temperature increase is expected. The double side thermal path can be seen in Figure 5.39.

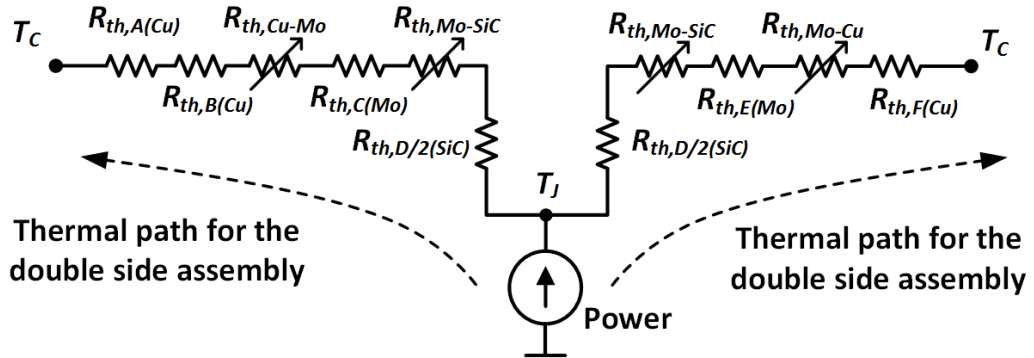


Figure 5.39 Equivalent thermal resistances and thermal path for the double side assembly

Using molybdenum contacts and the clamp rated at 400 N, the junction temperature rise has been characterised for different heating currents, as it was done for the single side cooling assembly. The results are presented in Figure 5.40, where they are compared with the large heatsink assembly. It can be clearly appreciated the reduction of the junction temperature increase.

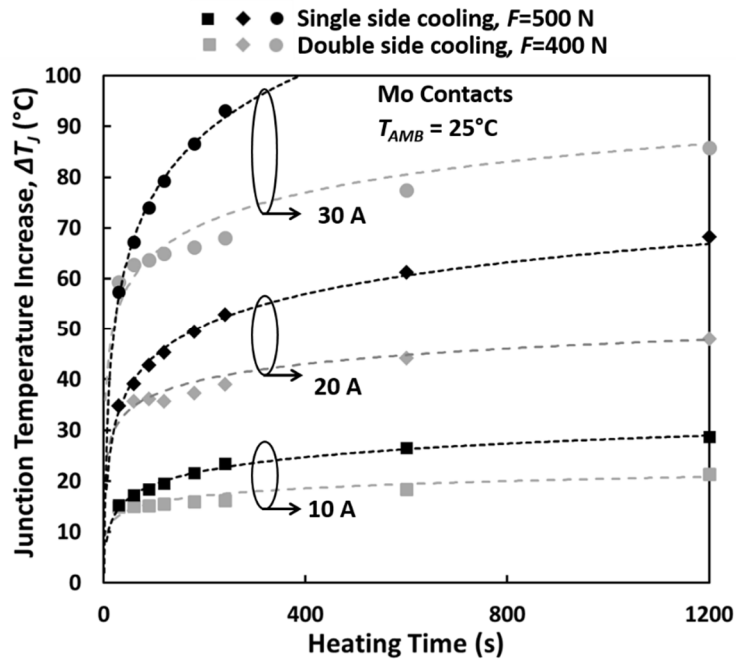


Figure 5.40 Impact of double side cooling on the transient heating. Molybdenum contacts

5.4 Power cycling performance of SiC diodes using pressure contacts

As it was mentioned in chapter 1, the degradation of the solder is one of the usual failure mechanisms of a solder based package system during power cycling, which causes an increase of the thermal resistance. In the case of press-pack assemblies, the lack of solder suggests a better thermal cycling performance hence, in order to verify this, a SiC Schottky diode in a TO-247 package, will be subjected to the same power cycle than the assembly using pressure contacts.

As it was already mentioned in chapter 1, some researchers [42, 43] use changes in the structure functions to identify the degradation of the packaging. Comparing the thermal resistances of the selected discrete device, (a 1700 V/26 A SiC Schottky diode from Cree/Wolfspeed with datasheet number C3D25170H which was characterised in chapter 1) with the press-pack prototype (analysed in sections 5.3.1. and 5.3.2 of this chapter) it is clearly observed how the thermal resistance is higher when pressure contacts are used. This will be compared clearly when the power cycling results are shown together later on in this section.

This higher value of the thermal resistance for the press-pack diode prototype compared with the solder based TO-247 has been explained in section 5.3.1: the addition of the thermal contact resistances, the influence of the single side cooling and the non-optimised thermal path due to the existence of a protruding section were the reasons which explained the higher thermal resistance. The approach of sintering the interface of semiconductor to one of the intermediate contacts has already been proposed [2, 44], The characterisation of the thermal resistance of a Si IGBT device using pressure contacts and sintering the collector contact to the IGBT using nano-silver has recently been presented in [45] reporting an improvement of 18.8%, however, given the reliability limitations of the solder layer for SiC devices [25, 26], the reliability and performance under power cycling of this proposed technique should be fully understood and characterised for silicon and SiC devices.

The discrete SiC device was subjected to power cycling using a heating current of 30 A for 30 s with a cooling time of 30 s. In this accelerated degradation tests, as defined in chapter 1, the number of cycles to failure is inversely proportional to the junction temperature excursion (ΔT_j) and for this particular test, the resulting ΔT_j was 53.1 °C, with

a maximum temperature of 96.6 °C. The transient thermal impedance was characterised every 200 cycles and the measured thermal resistance (R_{TH}) and forward voltage (V_F) across the diode during the power cycling tests are shown in Figure 5.41. From these results, it can be observed that for this test there was no observable thermal impedance degradation during power cycling. However, the final result of this experiment is a sudden failure after 19000 cycles. The forward voltage was characterised during the cycling process and an 18% increase in the forward voltage was observed at the point of failure. The spikes shown on the forward voltage in Figure 5.41 are due to the thermal impedance characterisation which occurs every 200 cycles. The temperature variation between night and day causes the low frequency oscillation.

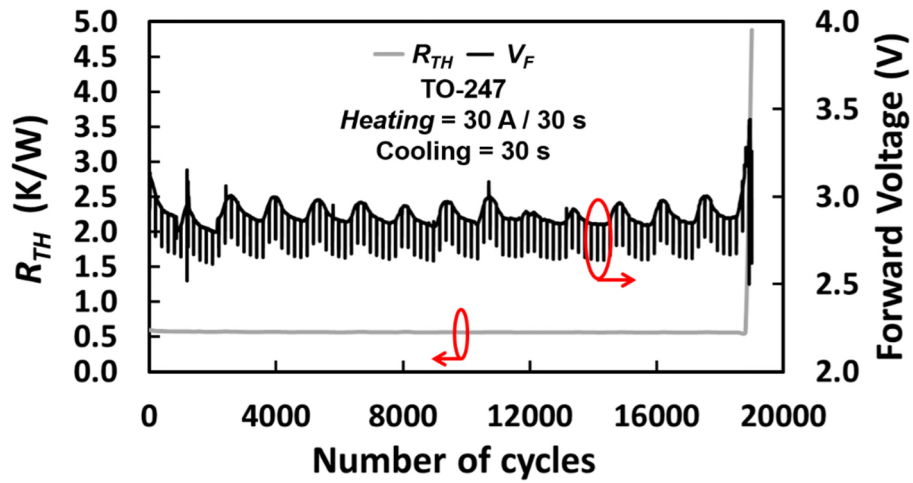


Figure 5.41 Thermal resistance and forward voltage during power cycling of the SiC Schottky diode in TO-247 package.

The same power cycling test was performed for the press-pack assembly using molybdenum and ALG contacts using the assembly presented in Figure 5.42, using a box clamp BX42 rated at 400 N. The power cycling test is based on using the same heating pulse for both packaging technologies namely a 30 A heating current during 30 seconds, with a 30 seconds cooling period.

The power cycling tests were performed at the University of Nottingham, where special thermal characterisation and power cycling equipment [36] is available.

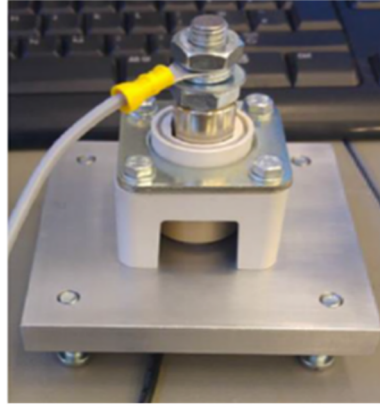


Figure 5.42 Picture of the SiC pressure package assembly connected for power cycling

The resulting junction temperature excursion ΔT_j for the assembly using the intermediate molybdenum contacts was 78.1 °C, with a maximum temperature T_{j-max} of 118.5 °C, while in the case of the ALG intermediate contacts, the resulting temperatures were a ΔT_j of 75.5 °C and a maximum temperature T_{j-max} of 113.7 °C. In both cases the cycling temperatures are higher than the TO-247 power cycling test. The power cycling results are summarised in Table 5-VI, with the medium junction temperature calculated as defined in chapter 1.

Table 5-VI Temperatures during the power cycling tests (single side cooling) for the three devices evaluated

	TO-247	Press-Pack Molybdenum	Press-Pack ALG
Junction temperature excursion, ΔT_j (°C)	53.1	78.1	75.5
Maximum Junction Temperature, T_{j-max} (°C)	96.6	118.5	113.7
Medium Junction Temperature, T_m (°C)	70.1	79.5	76.0

Figure 5.43 shows the temperatures during the power cycling of the press-pack assembly using ALG contacts, from cycle number 10000 to 15000. The spikes during the thermal impedance characterisation are clearly observed, together the low frequency oscillations caused by the temperature variation between day and night.

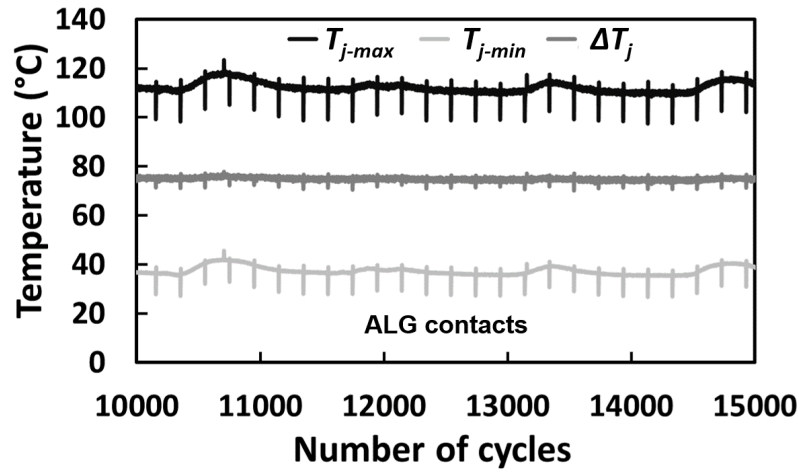


Figure 5.43 Junction temperatures during cycling of the ALG assembly. T_{j-max} , T_{j-min} and ΔT_j

As it was mentioned before, the transient thermal impedance was characterised every 200 cycles for both contact materials. The measured thermal resistances are shown in Figure 5.44, where they are compared with the thermal resistance of the discrete TO-247 device.

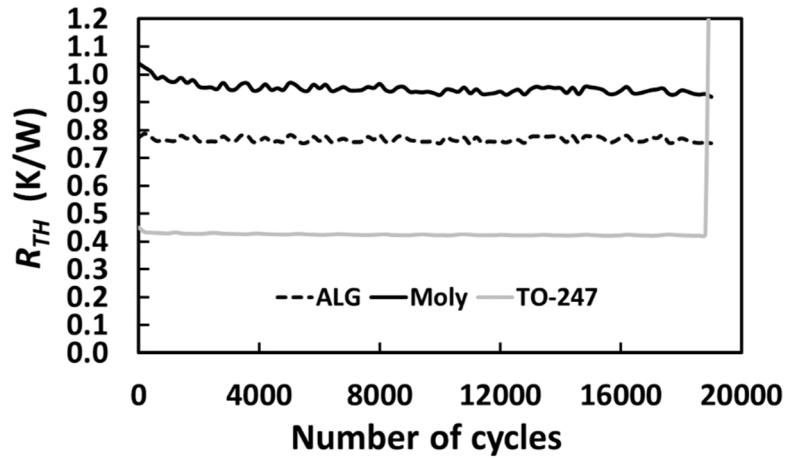


Figure 5.44 Evolution of the thermal resistances during power cycling of the different packaging technologies

Analysing the results presented, both pressure contact assemblies pass the number of cycles which triggered failure in the TO-247 package. This is despite the higher junction temperature excursion and the higher maximum junction temperature in the press-pack prototype. The plot of the thermal resistances as a function of the number of cycles presented in Figure 5.44 shows no overall increase in the thermal resistance during the power cycling of both prototypes using pressure contacts, although there is periodic

variation in the values. This is clearly appreciated in Figure 5.45, where the scale of the thermal resistance has been modified for a better analysis.

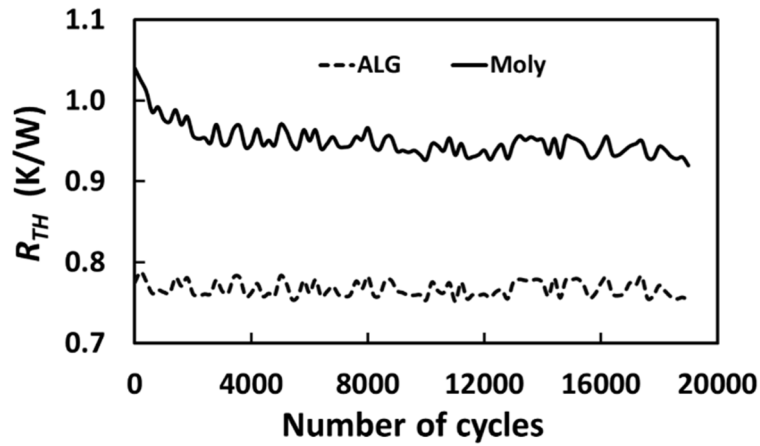


Figure 5.45 Thermal resistance during power cycling of the press-pack prototypes. ALG and Molybdenum

This variation is due to changes in the pressure at the interfaces during the power cycling, which is inevitable because of continuous expansion/contraction of the die and intermediate contacts, together with the deformation of the mechanical elements, which can lead to a non-uniform force distribution, as it is shown in Figure 5.46.

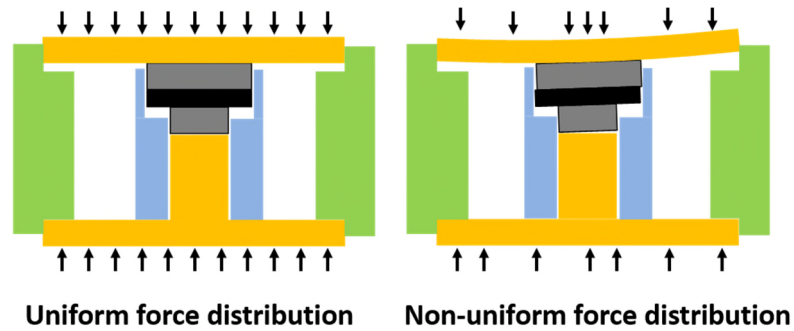


Figure 5.46 Representation of the impact of the uniformity of the force distribution and mechanical deformation in a press-pack module assembly

In the case of multichip chip modules, reduced contact force on individual chips during power cycling was identified in [46] as a possible failure mechanism of press-pack IGBT modules. Pressure imbalance appears as an added variable to the problem of paralleling multiple chips. Moreover, as was mentioned previously, the press-pack assemblies require a more complex mechanical system that is used to apply an external force to achieve perpendicular and equally distributed force across the whole surface of the module. Temperature variations can also affect the clamping system leading to a non-

equally distributed force, which would have considerable impact on multiple chip modules, hence, the impact of pressure imbalance in multichip SiC Schottky diode modules using pressure contacts is evaluated in the next section.

5.5 Impact of pressure non-uniformity on multichip press-pack diodes

If SiC devices are to be used in press-pack applications, then high current multichip assemblies are inevitable. Hence, a 200 A SiC Schottky diode press-pack module was designed and assembled. Figure 5.47 shows a 3D model of the prototype, while Figure 5.48 presents the multichip diode during different stages of the assembly. The design of the multichip diode is based on the single chip module, sharing the external dimensions, as it can be seen in Figure 5.48. The technical drawings are presented in Annex A of this thesis.

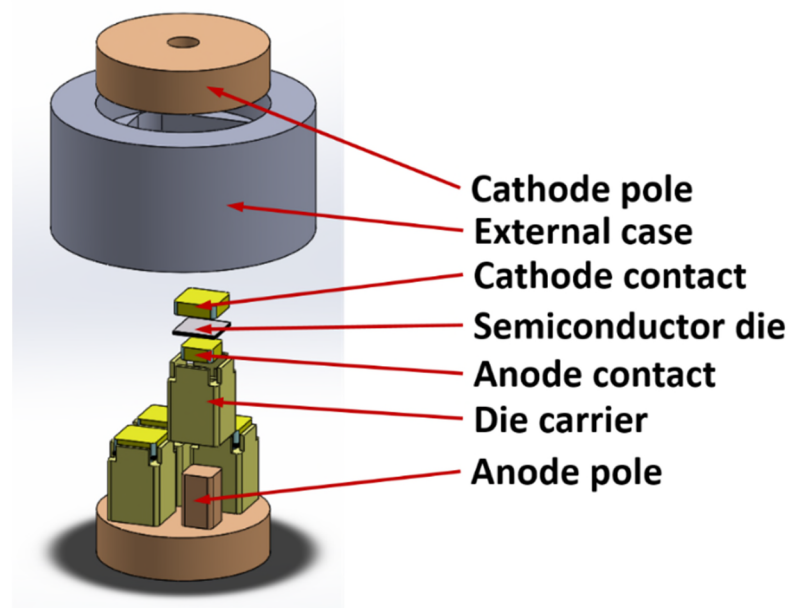


Figure 5.47 3D Model of the multichip diode module

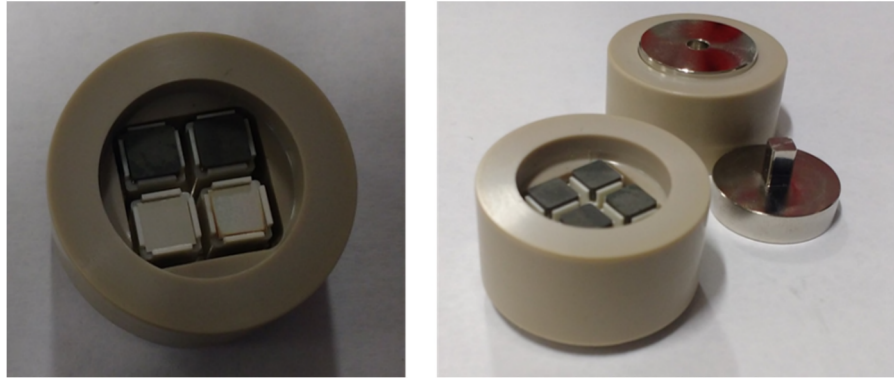


Figure 5.48 Different stages of the assembly of the multichip diode using pressure contacts

In multi-chip modules, maintaining equal pressures across all chips is critical for ensuring optimal current sharing between the parallel devices. In large area devices like thyristor wafers, unequal pressure over the area of the device will lead to hotspots on the wafer. In the case of multi-chip press-pack power modules, devices with lower contact force will exhibit higher junction to case thermal resistance and higher electrical resistance thereby diverting current to devices with higher contact force. Commercially available press-pack IGBTs have been designed using two techniques. Using individual springs for each chip [13, 23] or applying a common force which will be equally distributed between the chips of the module [14].

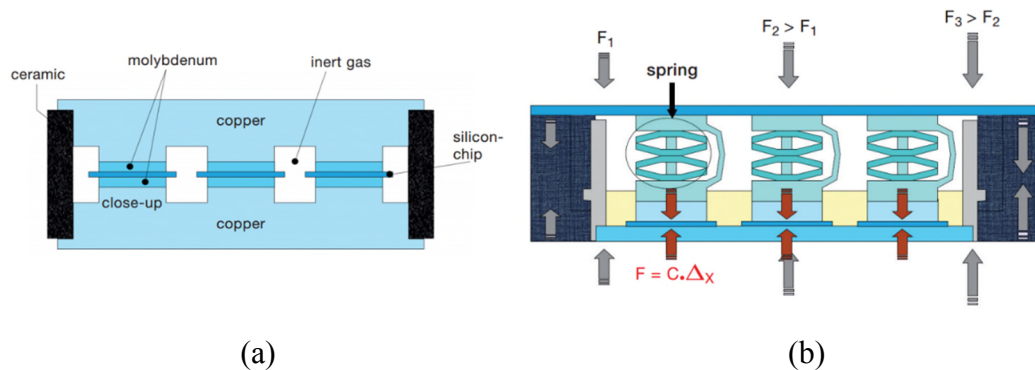


Figure 5.49 (a) Press-pack module where a common force is applied to all the chips [23] (b) Press-pack module where an individual spring contact is used for applying the force on each chip [23]

In the design based on individual springs for maintaining the pressure on each chip (ABB Stakpak), the force on the chip F is determined by the product of the spring constant C and the distance travelled by the spring Δx , with the excess of force absorbed by the package. In both designs, unequal pressure will lead to current imbalance and reduced reliability, however the solution based on the individual spring for each chip

would be more immune to the dimensional tolerances of the elements of the assembly and to the thermal deformations. The designed prototype is based in the common force approach, and the pressure is maintained by a global contact common to all devices as shown in Figure 5.50. It can be seen from Figure 5.51 that reduced pressure and loss of contact is possible if there is mechanical deformation in one or both common pole contacts. The mechanical deformation will lead to higher contact resistances, hence, current imbalance between the paralleled chips.



Figure 5.50: Multichip press-pack module without mechanical deformation and optimal force distribution)

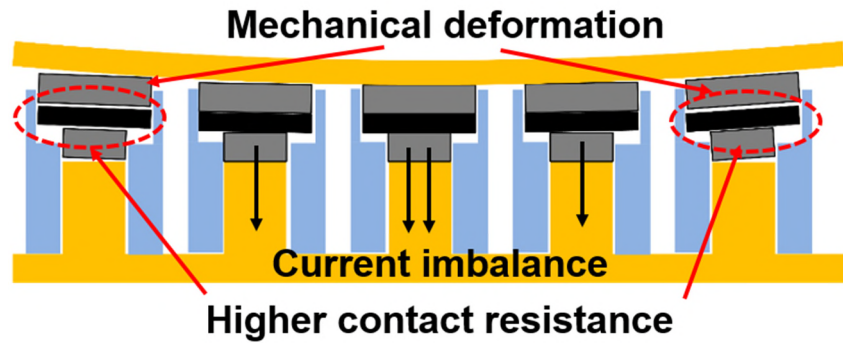


Figure 5.51 Multichip press-pack module with mechanical deformation (unequal force distribution)

5.5.1 Electrothermal characterisation of a multiple chip press-pack module

The evaluation of the electrical characteristics of the multichip module has been done using the test configuration defined in section 5.3.2, using a box clamp rated at 500 N and a box clamp rated at 2000 N. Assuming equal distribution of forces among the parallel chips, the clamping forces are 125 N/chip and 500 N/chip respectively. For these studies, molybdenum has been selected as intermediate contact material.

The forward voltage was captured for 15 s pulses at different DC currents and the results are presented in Figure 5.52. From the results shown in Figure 5.52, it is observed

that the forward voltage increases with increasing current and it is higher for the lower clamping force. The currents are below the zero temperature coefficient, hence the decreasing voltage during the duration of the heating pulse.

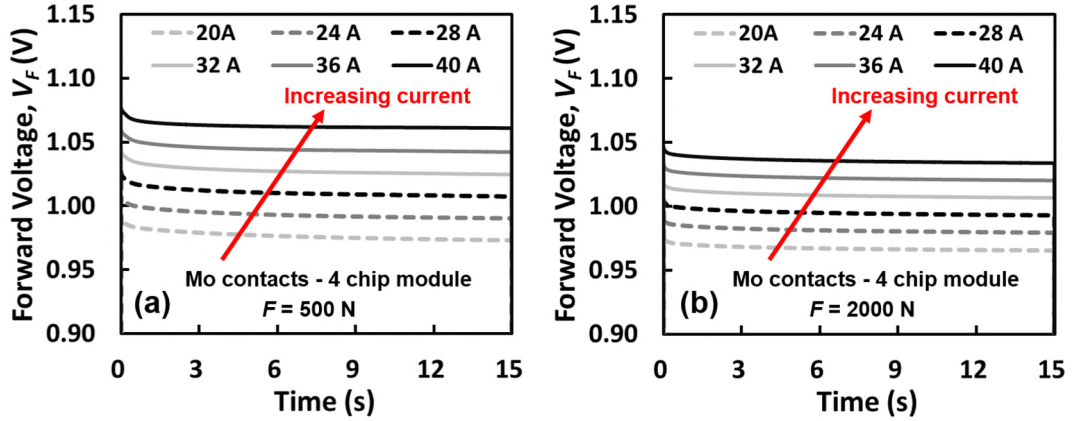


Figure 5.52 Characterisation of the forward voltage of the multi-chip module for different DC current pulses. (a) $F = 500$ N (b) $F = 2000$ N

The impact of the clamping force on the forward voltage is clearly observed in Figure 5.53(a), where the forward voltages for the same current and clamping forces of 500 N and 2000 N are compared in the same graph. An initial steep change in the forward voltage is observed for the lower clamping force, indicating a fast temperature increase. Figure 5.53(b) compares the measured forward voltage for a single chip module and a clamping force of 500 N, with the measured forward voltage for a multichip module and a clamping force of 2000 N. A minimal difference between forward voltages can be observed, hence the effective individual clamping force can be identified as 500 N.

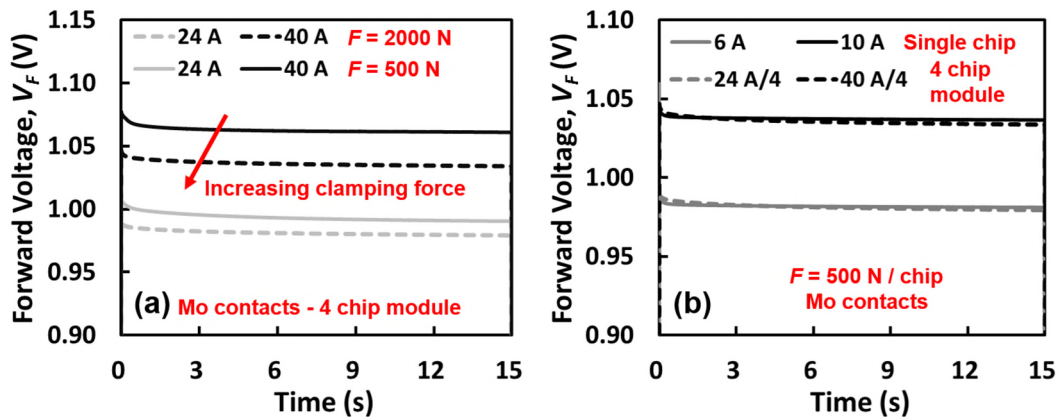


Figure 5.53 (a) Impact of the clamping force on the forward voltage during a DC pulse for a multi-chip module, (b) Forward voltage during a DC pulse for single chip and multi-chip modules for an effective clamping force of 500 N

In the measurements shown previously, the clamp was properly adjusted, allowing the assumption of equal force distribution between chips. However, as the power cycling results in section 5.4 have shown, the force distribution can have an impact on the performance of multiple chip press-pack modules.

The reduced clamping force can be emulated if the bolts of the BX42 clamp are not uniformly tightened. Starting from a loose clamp, the forward voltage at different stages of the tightening procedure is shown in Figure 5.54. It is clearly observed how the forward voltage is higher for a lower clamping force (i.e. loose clamp) while for a proper tightened clamp the forward voltage is low. The load current used for this test was 40 A, which in case of equal current sharing should be below the ZTC, hence the forward voltage should decrease slightly during the self-heating of the diode, as the self-heating at this current level is low.

It is clearly observed how the forward voltage is higher at low clamping forces, due to the higher contact resistances. The forward voltage can be an indicator of uneven current sharing for load currents below the ZTC, with the higher voltage as an indicator of a global increase in the contact resistance. The change in the slope for the voltage during self-heating can also identify current imbalance between chips. In the case of the loose clamp, the forward voltage increases after an initial steep dip in the forward voltage, clearly an indicator of a clamping force imbalance between the paralleled chips.

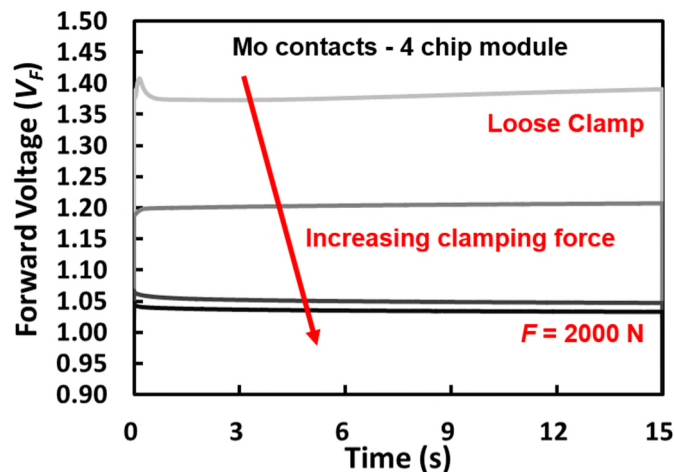


Figure 5.54 Forward voltage of a multi-chip diode during a heating pulse at different stages of the assembly/tightening of the clamp.

In order to study how the pressure imbalance affects the current distribution and the forward voltage, the test configuration used previously in section 5.3.2 was adapted

for using 2 press-pack modules in parallel. This study was performed using a single chip module on each clamp and the modified electrical schematic is shown in Figure 5.55(a) while the connection of the two diodes is shown in Figure 5.55(b), where the heatsink PS136/150 is also shown. Diodes with similar forward voltages were selected for paralleling, but it is important to mention that there are multiple factors that will affect the forward voltage of the assembly, like the mechanical tolerances, flatness and roughness of the surfaces in contact, highlighting the importance of the mechanical assembly for press-pack modules.

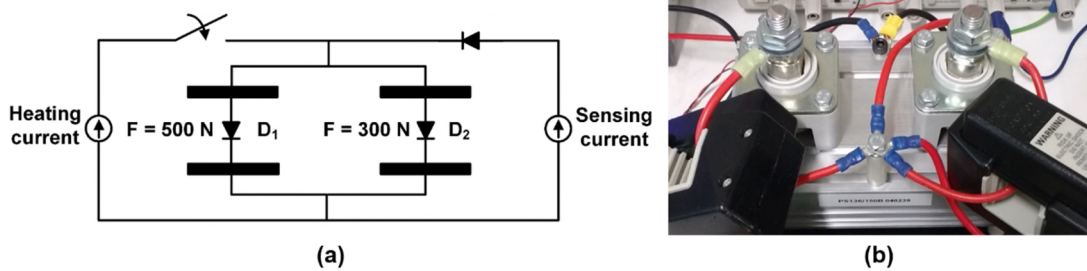


Figure 5.55 (a) Electrical schematic and (b) detail of the connection of the two box clamps on the heatsink PS136/150B for the pressure imbalance tests

Tektronix current probes model TCP303 were connected to each press-pack module to measure the current through each diode. Two scenarios were evaluated in case of imbalance of the clamping force: case A where both clamps are completely tight and the clamping forces are the nominal values, namely $F_{D1}=500\text{N}$ and $F_{D2}=300 \text{ N}$, and case B, where the 4 bolts of the clamp of D_2 were tightened by hand thereby resulting in a clamping force lower than 300 N, as the spring compression is less than its nominal value. The first case is a mild case of pressure imbalance whereas the second case is more severe.

DC heating pulses of 10 A and 40 A with a duration of 300 seconds were used to evaluate the impact of the pressure imbalance on current distribution between the two parallel diodes, for the two clamping scenarios described previously

- A) Clamping force imbalance 300 N/ 500 N
- B) Clamping force imbalance 500 N / loose clamp.

As in the case of traditional wire bonded modules, the point of operation will have an impact on the electrothermal equilibrium of the paralleled diodes [47]. When the load

current is below the ZTC, for the case of a mild pressure imbalance, it can be concluded that the low self-heating has not a significant impact on the current distribution, as the results in Figure 5.56 show.

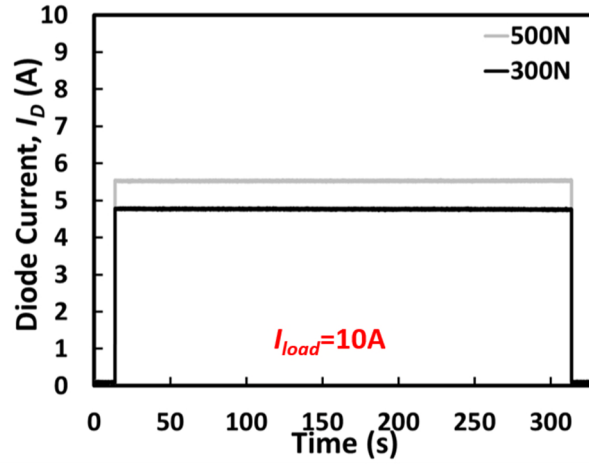


Figure 5.56 Current distribution for a load current of 10 A. Low pressure imbalance

If the pressure imbalance increases, from the results presented in Figure 5.57 it can be observed that the ratio between both currents increases considerably and a slight change in the current distribution with temperature can be observed, as the current through the device which conducts the majority of the current slightly reduces. This current is below the ZTC and the slight reduction can be attributed to the increase of resistance of the intermediate contacts with temperature.

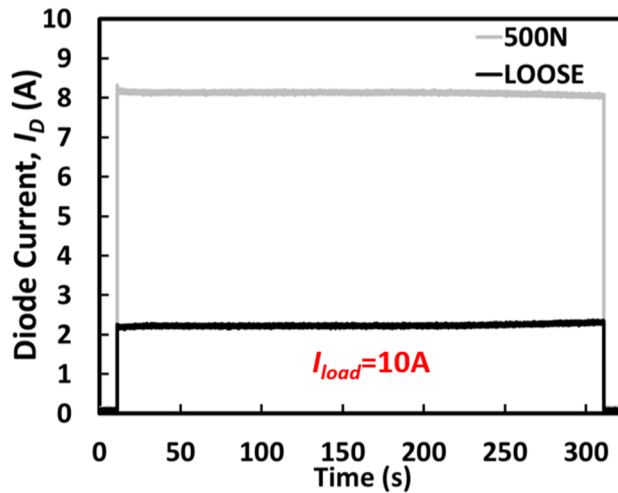


Figure 5.57 Current distribution for a load current of 10 A. High pressure imbalance

For a current level above the ZTC, namely 40 A, and a small pressure imbalance,

the currents converge as the device conducting more current increases its temperature due to the self-heating, as the results on Figure 5.58 show.

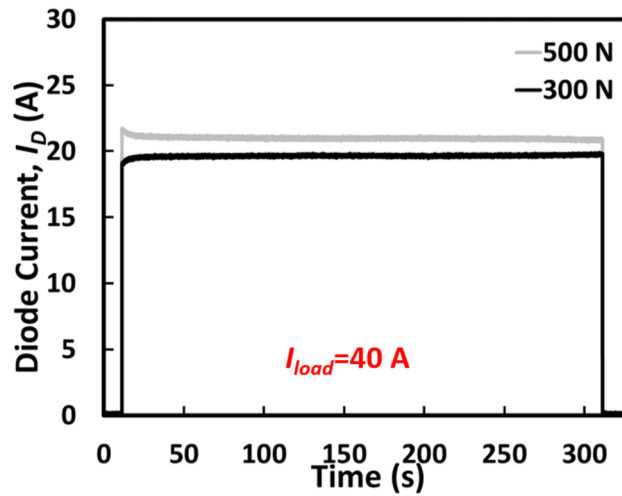


Figure 5.58 Current distribution for a load current of 40 A. Low pressure imbalance

For a high pressure imbalance, Figure 5.59 shows a considerable difference in the shared current as in the case of the 10 A load current. The thermal response to the initial current imbalance causes an initial dip in the current through the device properly clamped and as the diode which carries more current increases its temperature, the currents converge due to the positive temperature coefficient of the Schottky diodes at that current level.

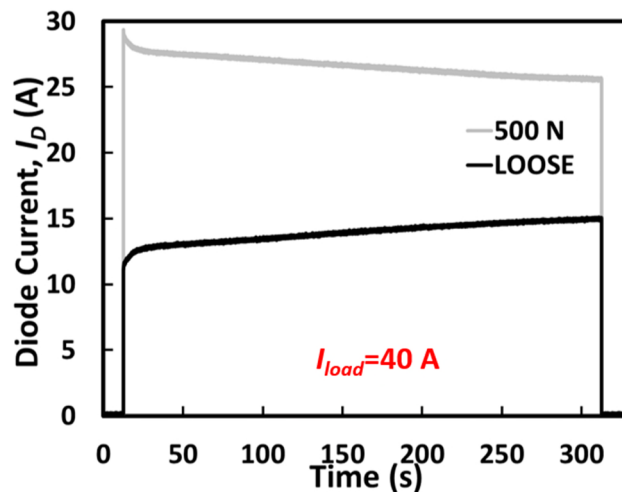


Figure 5.59 Current distribution for a load current of 40 A. High pressure imbalance

Evaluating the on-state voltage for the parallel diodes in the cases of clamping force imbalance, from Figure 5.60 it can be seen that for both 10 A and 40 A load currents, the pressure imbalance leads to a higher voltage, hence causing a higher power dissipation.

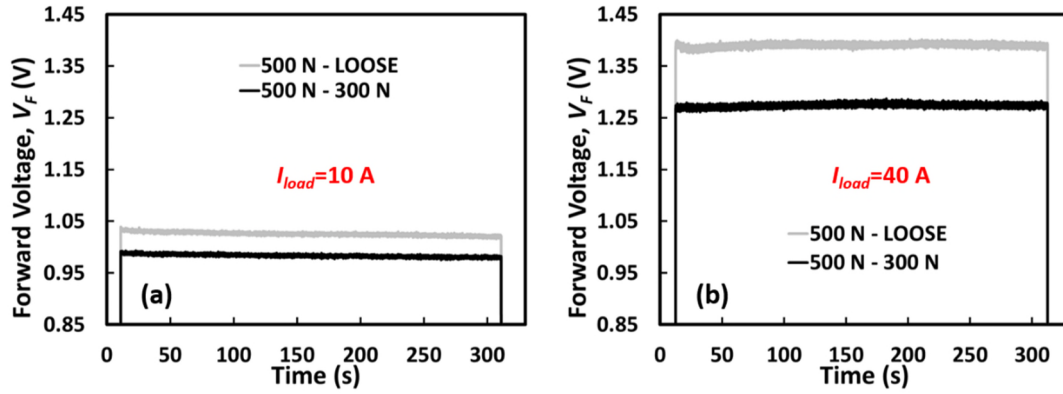


Figure 5.60 Forward voltage as a result of the pressure imbalance. (a) Load current 10 A DC, (b) Load current 40 A DC.

Analysing Figure 5.60(a) in the case of the load current of 10 A, as the value is below the ZTC, the forward voltage decreases during the self-heating, whereas in the case of the 40 A load current, shown in Figure 5.60(b), an initial dip is observed in the high pressure imbalance. This initial dip, caused by the transient response to the current imbalance, could be an indicator of loss of pressure, as the load current is above the ZTC.

During the tests performed for the evaluation of the clamping force imbalance, the test setup shown in Figure 5.55(a) was used and a sensing current of sensing current of 200 mA was passed through the parallel press-pack devices. The individual currents were captured at ambient temperature (25 °C) using the Tektronix TCP303 current probes.

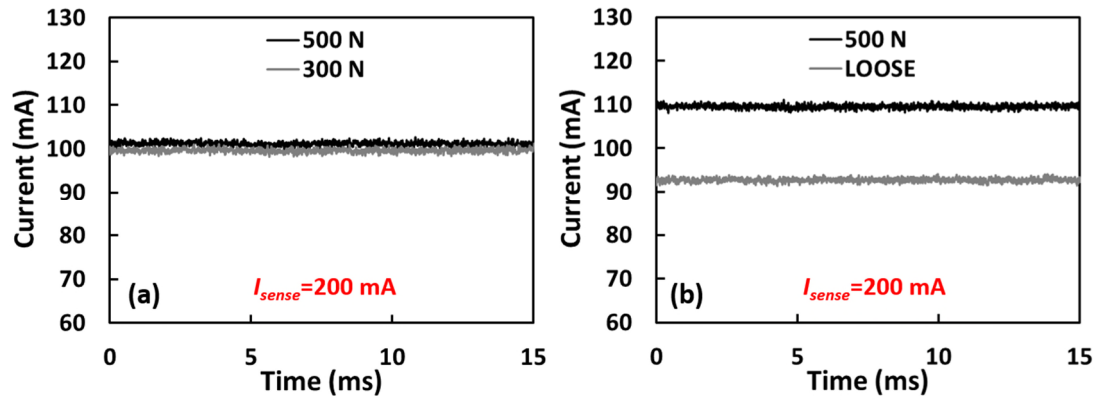


Figure 5.61 Sensing current distribution waveforms: (a) 500 N/300N imbalance (b) 500 N / LOOSE clamp imbalance

The measured sensing current values through each diode are presented in Table 5-VII where it can be seen that the device with the higher clamping force conducts more current, as expected. The current disparity is proportional to the pressure disparity since the more severe case of pressure imbalance leads to a higher current imbalance. The unequal current distribution would have an impact on the junction temperature estimation, as it was discussed on chapter 4.

Table 5-VII: Impact of the clamping force imbalance on the sensing current distribution

Clamping Forces	I_{D1} (mA)	I_{D2} (mA)
$F_{D1} = 500 \text{ N} / F_{D2} = 300 \text{ N}$	101.2	99.7
$F_{D1} = 500 \text{ N} / F_{D2} = \text{loose clamp}$	109.6	92.7

Current press-pack IGBT modules use Si PiN diodes to enable reverse conduction. In silicon PiN diodes, the increase in minority carrier lifetime with temperature creates a higher carrier density in the drift region which causes the ZTC point to be higher compared to SiC Schottky diodes which are unipolar [48].

Current sharing between parallel diodes during on-state was evaluated for silicon PiN diodes by passing a DC current of 4 A through the parallel connection of two 600 V/4 A Si PiN diodes with datasheet reference HFA04TB60. A variation in the thermal resistance between the parallel pair, meant to emulate degradation like solder voiding in a traditional package or loss of force contact in press-pack packaging, was introduced to investigate how current imbalance occurs. Figure 5.62 shows the measured currents during a 20 s/4 A heating pulse for the parallel diodes.

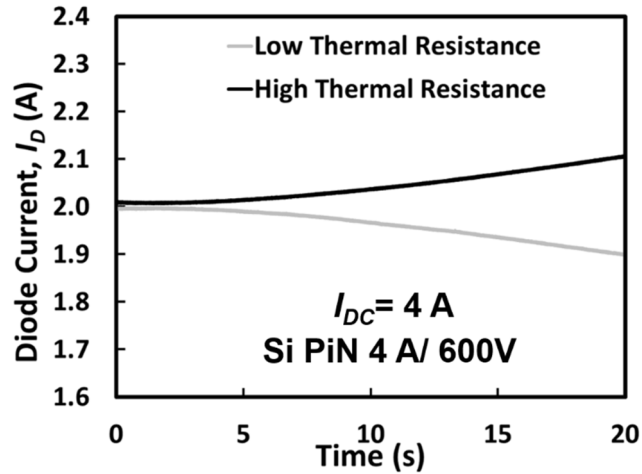


Figure 5.62 Current distribution for parallel silicon PiN diodes with electrothermal imbalance

As it can be seen in Figure 5.62, the higher ZTC causes the hotter device, which has a higher thermal resistance, to conduct more current, hence the currents diverge, increasing the possibility of thermal runaway. However, as it was shown previously, in the case of a multi-chip SiC Schottky diode using pressure contacts, loss of pressure uniformity causes current imbalance. Nevertheless, the lower ZTC makes this imbalance electrothermally stable.

The better performance of SiC Schottky diodes under pressure imbalance when devices are paralleled, in addition to the superior switching properties of SiC devices [47], suggest that hybrid press-pack Si IGBT modules with SiC Schottky diodes can be a suitable packaging alternative.

The change in the current distribution between the chips in the module, together with the on-state voltage, can be used for monitoring the pressure imbalance between chips. Current sensors distributed within the module, which would monitor the current through the chips can be used for inferring the pressure distribution. It can be done at low currents, as the results on Table 5-VII suggest or at higher currents during operation. The identification of the junction temperature for a multichip press-pack assembly using the on-state voltage at low currents would be challenging, as the results on chapter 4 indicate, given that the sensing current distribution would be affected by both the temperature difference between the chips and the differential electrical contact resistance.

5.6 Summary

In this chapter the design, development and testing of silicon carbide Schottky diodes in a press-pack assembly has been performed.

Using a single chip prototype, the impact of the clamping force and the intermediate contact material on the thermal and electrical properties. The results show that the choice of contact material is critical. Compared with the molybdenum, the studies presented indicate that the press-pack prototype with Aluminium Graphite contacts exhibits a lower junction temperature excursion despite having a higher on-state voltage caused by the higher electrical resistivity of ALG.

It means that for the same power ALG press-pack design can be smaller (by reducing the size of the heatsink for example), or the clamping force can be reduced. Double side cooling, at a reduced clamping force, improves the cooling of the diode and a lower operating junction temperature is achieved with reduced mechanical stresses on the diode. The presented prototype has not been optimised for thermal performance, especially when it is compared with a traditional solder based module, where the thermal contact resistances are removed.

Power cycling tests have been performed using intermediate contacts of ALG and molybdenum and both assemblies pass the test which caused the failure of a SiC device in a TO-247 package. Despite having a higher maximum junction temperature and junction temperature excursion, both press-pack assemblies passed the test.

During the power cycling tests, variations of the thermal resistance were observed for both contact materials. This variation is caused by the expansion/contraction of the elements of the packaging and has an impact on the contact resistances of the module. In the case of a multiple chip module it will cause a differential thermal resistance between the parallel chips.

The impact of clamping force imbalance between parallel chips was studied for SiC Schottky diodes. It is shown that the lower ZTC in SiC Schottky diodes compared to silicon PiN diodes means that in the case of current imbalance resulting from the loss of pressure uniformity, the system will be electrothermally stable.

A multiple chip module was designed, assembled and characterised. Following the results obtained, in the case of multiple chip modules using pressure contacts, the current sharing between chips and the forward voltage, could be suitable health indicators for pressure packaging assemblies.

5.7 References

- [1] S. Klaka. *Thyristors – The heart of HVDC*. Available: <https://www.abb-conversations.com/2015/11/thyristors-the-heart-of-hvdc/> (Access: 9/05/2017).
- [2] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2011.
- [3] Schunk Hoffmann Carbon Technology AG. - *Thermal Management: Aluminium Graphite Discs & Rings*. Available: <http://www.hoffmann.at/en/hos/DiscsRings/schunk01.c.79396.en> (Access: 7/06/2017).
- [4] Infineon. *IGBT Modules up to 4500V / 6500V*. Available: <http://www.infineon.com/cms/en/product/power/igbt/igbt-module/igbt-module-4500v-6500v/channel.html?channel=ff80808112ab681d0112ab69f8450396> (Access: 07/06/2017).
- [5] ABB. *Insulated gate bipolar transistor (IGBT) and diode modules with SPT and SPT+ chips*. Available: <http://new.abb.com/semiconductors/igbt-and-diode-modules> (Access: 7/06/2017).
- [6] Mitsubishi. *HVIGBT Modules/HVIPM*. Available: <http://www.mitsubishielectric.com/semiconductors/products/powermod/hvigbtmod/> (Access: 7/06/2017).
- [7] N. Kirby, "HVDC Technology - Voltage Source Converters," presented at the IEEE PES T&D Expo, Chicago, 2014.
- [8] ABB, "HVDC Light. It is time to connect," ed: ABB, 2012.
- [9] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, and D. Soerangr, "HVDC PLUS – Basics and Principle of Operation," ed: Siemens AG, 2009.
- [10] GE-Alstom. *HVDC MaxSine™*. Available: <http://www.gegridsolutions.com/alstomenergy/grid/products-services/product-catalogue/electrical-grid-new/hvdc/hvdc-solutions/hvdc-maxsinetm/index.html> (Access: 13/06/2017).
- [11] K. Eriksson, "HVDC Light and development of Voltage Source Converters," presented at the IEEE/PES T & D Latin American Conference, Sao Paulo, Brazil, 2002.

- [12] E. Mircea, L. Chen-Ching, and E. Abdel-Aty, "Power Semiconductor Devices for HvdC and Facts Systems," in *Advanced Solutions in Power Systems:HVDC, FACTS, and Artificial Intelligence*, ed: Wiley-IEEE Press, 2016, p. 1072.
- [13] S. Eicher, M. Rahimo, E. Tsyplakov, D. Schneider, A. Kopta, U. Schlapbach, *et al.*, "4.5kV press pack IGBT designed for ruggedness and reliability," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, pp. 1534-1539 vol.3.
- [14] F. Wakeman, K. Billett, R. Irons, and M. Evans, "Electromechanical characteristics of a bondless pressure contact IGBT," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, 1999, pp. 312-317 vol.1.
- [15] I. Omura, T. Domon, E. Miyake, Y. Sakiyama, T. Ogura, M. Hiyoshi, *et al.*, "Electrical and mechanical package design for 4.5kV ultra high power IEGT with 6kA turn-off capability," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 114-117.
- [16] T. Fujii, K. Yoshikawa, T. Koga, A. Nishiura, Y. Takahashi, H. Kakiki, *et al.*, "4.5 kV-2000 A Power Pack IGBT (ultra high power flat-packaged PT type RC-IGBT)," in *12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No.00CH37094)*, 2000, pp. 33-36.
- [17] A. Petterteig, R. Pittini, M. Hernes, and O. Holt, "Pressure tolerant power IGBTs for subsea applications," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1-10.
- [18] S. Gunturi and D. Schneider, "On the operation of a press pack IGBT module under short circuit conditions," *IEEE Transactions on Advanced Packaging*, vol. 29, no. 3, pp. 433-440, 2006.
- [19] P. Bill, A. Welleman, E. Ramezani, S. Gekenidis, and R. Leutwyler, "Novel press pack IGBT device and switch assembly for Pulse Modulators," in *2011 IEEE Pulsed Power Conference*, 2011, pp. 1120-1123.
- [20] J. Schuderer, U. Drogenik, B. Agostini, F. Brem, F. Mohn, and F. Canales, "Challenges and new approaches for power module's next generation packaging technology," presented at the IMAPS From Nano to Micro Power Electronics and Packaging Workshop, 2013.
- [21] F. Wakeman, "Press-pack IGBT, towards the next generation of super switch," presented at the Power Electronics Event, Delft, 2014.
- [22] I. Westode, "Press-Pack IGBT 3-Level Inverters Product Brief," ed, 2014.
- [23] ABB, "StakPak IGBT press-pack modules Flyer," ed, 2015.
- [24] R. Jakob, C. Keller, G. Mohlenkamp, and B. Gollentz, "3-Level high power converter with press pack IGBT," in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1-7.
- [25] C. Herold, M. Schaefer, F. Sauerland, T. Poller, J. Lutz, and O. Schilling, "Power cycling capability of Modules with SiC-Diodes," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-6.

- [26] L. A. Navarro, X. Perpiñà, P. Godignon, J. Montserrat, V. Banu, M. Vellvehi, *et al.*, "Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap Semiconductor Devices and Harsh Environment Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2261-2271, 2014.
- [27] Y. Sugawara, S. Ogata, S. Okada, T. Izumi, Y. Miyanagi, K. Asano, *et al.*, "4.5 kV 1000 A Class SiC pn Diode Modules with Resin Mold Package and Ceramic Flat Package," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*, 2008, pp. 267-270.
- [28] Y. Sugawara, D. Takayama, K. Asano, S. Ryu, A. Miyauchi, S. Ogata, *et al.*, "4H-SiC high power SIJFET module," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 127-130.
- [29] V. Banu, P. Godignon, X. Jordà, M. Alexandru, and J. Millán, "SiC Schottky Diode surge current analysis and application design using behavioral SPICE models," in *CAS 2012 (International Semiconductor Conference)*, 2012, pp. 359-362.
- [30] V. Banu, P. Godignon, X. Perpiñà, X. Jordà, and J. Millán, "Enhanced power cycling capability of SiC Schottky diodes using press pack contacts," *Microelectronics Reliability*, vol. 52, no. 9, pp. 2250-2255, 2012/09/01/ 2012.
- [31] M. Loboda. *Considerations for designing power electronic devices based on advanced SiC technologies.* Available: <http://www.dowcorning.com/content/publishedlit/11-3382-01.pdf> (Access: 3/05/2017).
- [32] Andreas Volke and M. Hornkamp, *IGBT modules. Technologies, driver and application*, Second ed.: Infineon Technologies AG, 2012.
- [33] Roechling. *Sustatron PPS.* Available: <https://www.roechling.com/industrial/materials/thermoplastics/detail/sustatron-pps-240/> (Access: 27/06/2017).
- [34] Roechling. *Sustapeek.* Available: <https://www.roechling.com/industrial/materials/thermoplastics/detail/sustapeek-196/> (Access: 27/06/2017).
- [35] *GD Rectifiers.* Available: <http://www.gdirectifiers.co.uk/> (Access: 27/06/2017).
- [36] Mentor. *Mentor Graphics T3ster.* Available: <https://www.mentor.com/products/mechanical/micred/t3ster/> (Access: 26/06/2017).
- [37] A. A. Hasmasan, C. Busca, R. Teodorescu, L. Helle, and F. Blaabjerg, "Electro-Thermo-Mechanical Analysis of High-Power Press-Pack Insulated Gate Bipolar Transistors under Various Mechanical Clamping Conditions," *IEEJ Journal of Industry Applications*, vol. 3, no. 3, pp. 192-197, 2014.
- [38] M. M. Yovanovich, "Four decades of research on thermal contact, gap, and joint resistance in microelectronics," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 2, pp. 182-206, 2005.
- [39] Schunk Hoffmann Carbon Technology, "Aluminium Graphite Composites. Product Information," 2016.

-
- [40] Schunk Hoffmann Carbon Technology "Aluminium Graphite Composites Thermal Management Materials for High Reliability Applications in Power Electronics," 2016.
 - [41] Bruker - *ContourGT-X 3D Optical Microscope*. Available: <https://www.bruker.com/products/surface-and-dimensional-analysis/3d-optical-microscopes/contourgt-x/overview.html> (Access: 27/06/2017).
 - [42] M. A. Eleffendi, L. Yang, P. Agyakwa, and C. Mark Johnson, "Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement," *Microelectronics Reliability*, vol. 59, pp. 73-83, 4// 2016.
 - [43] A. Aliyu and A. Castellazzi, "Prognostic System for Power Modules in Converter Systems Using Structure Function," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1-1, 2017.
 - [44] S. Steinhoff and P. Townsend, "Sintered backside shim in a press pack cassette," ed: Google Patents, 2015.
 - [45] E. Deng, Z. Zhao, P. Zhang, Y. Huang, and J. Li, "Optimization of the thermal contact resistance within press pack IGBTs," *Microelectronics Reliability*, vol. 69, pp. 17-28, 2// 2017.
 - [46] L. Tinschert, A. R. Årdal, T. Poller, M. Bohlländer, M. Hernes, and J. Lutz, "Possible failure modes in Press-Pack IGBTs," *Microelectronics Reliability*, vol. 55, no. 6, pp. 903-911, 2015/05/01/ 2015.
 - [47] J. Hu, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Comparative electrothermal analysis between SiC Schottky and silicon PiN diodes: Paralleling and thermal considerations," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1-8.
 - [48] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2008.

6 Conclusions

6.1 Introduction

This chapter summarises the main conclusions of the work performed in this thesis as well as provides guidance for further research on the topics of reliability, electrothermal characterisation of power devices and implementation of condition monitoring.

6.2 Conclusions

Identifying the junction temperature of power semiconductors using temperature sensitive electrical parameters (TSEPs) is one of the main techniques used for the implementation of condition monitoring strategies, as the junction temperature can be an indicator of degradation resulting from ageing damage of the power module. Moreover, condition monitoring can be used improving the lifetime of the module and defining operational constraints based on junction temperature.

SiC MOSFETs are now a mature technology, with different products available in the market as well as in research stage. However, the research on TSEPs for SiC devices is not as extensive as it is for silicon devices. The use of TSEPs for condition monitoring has made the electrothermal characterization of power devices and modules essential for effective implementation. Some classic TSEPs are well understood and are well-known (like the on-state voltage of an IGBT at low currents), however the emergence of new device technologies and new packaging methods makes the electrothermal characterisation even more relevant. This thesis has demonstrated that the different electrothermal characteristics of SiC power devices need to be taken into consideration for TSEP based condition monitoring to become a reality. This has been shown in the context of conventional discrete packaged power devices and press-pack devices.

6.3 Future Work

This thesis has laid the foundations of electrothermal characterisation and modelling of TSEPs for advanced power devices, however, areas of future work have been identified. In this thesis, the devices have been characterised up to temperatures of 150 °C, however given the ability of SiC to operate high temperatures and the emergence of high temperature packaging methods will make the electrothermal characterisation at high temperatures essential. The characteristics and performance of TSEPs at such temperatures need evaluation if condition monitoring is to be implemented in high temperature and harsh environment applications.

Another important point of future work is the reliability of the TSEP itself. From analysing the TSEPs identified for SiC MOSFETs in this thesis, namely the turn-on current switching rate (dI_{DS}/dt) and the gate current plateau (I_{GP}), it is clear that both are affected by the transconductance of the device and threshold voltage. However the transconductance and threshold voltage both depend on the integrity of the gate oxide. Gate oxides compromised by increased interface trap density and fixed oxide charge will exhibit increased gate leakage currents, unstable threshold voltage and reduced transconductance. The reliability gate oxide has been a major concern for SiC MOSFETs hence, the evaluation of the stability of the proposed TSEPs should be taken in to consideration for instances where the gate oxide may be compromised. It should be noted that in the case of a known temperature, the TSEPs could also be used as an indicator of oxide degradation.

Given the limitations in current conduction capability of SiC devices, paralleling of chips is a requirement for enabling high current capability. This would have an impact on the TSEP effectiveness, as it has been shown in chapter 4 of this thesis for Si PiN diodes and SiC Schottky diodes. Studying the effectiveness of proposed TSEPs for parallel MOSFETs and power modules should be the next research step. The potential for the TSEP to underestimate the junction temperature of potentially defective devices in parallel connection with healthier devices has been shown to be real in this thesis. Hence, ways of implementing condition monitoring techniques that do not just rely on averaging junction temperatures between parallel chips is needed, especially for packaging methods like pressure packaging.

GaN devices are even less technologically mature than SiC devices, hence, the reliability concerns are greater. Condition monitoring in GaN will be more complicated given the greater reliability concerns. For example, GaN FETs are typically fabricated on silicon substrates and since the semiconductors are not lattice matched, some intermediate layers comprising of crystal defects are needed as a buffer. The performance of these layers under temperature and power cycling has not been as extensively studied as has been the case with silicon and to a lesser extent SiC. Furthermore, the very low gate drive voltages and high susceptibility of electromagnetic emissions in GaN makes the temperature sensitivity of the device harder to detect. For enhancement mode GaN FETs, the reliability of the gate is a well-known operational concern given that the gates are not conventional MOS gates. Hence, condition monitoring of GaN devices in failure critical applications is clearly an area of future work.

The emergence of intelligent gate drivers and the ability to use these gate drivers for on-line condition monitoring using TSEPs is also an area of future work. Gate drivers with variable gate drive output impedances have been demonstrated for optimising the switching performance of wide bandgap devices by maximizing the switching rates without compromising EMI. Companies like AMANTYS have already demonstrated gate drives with 15 different output impedances that can be configured by the user. The design and implementation of such gate drivers for the purpose of implementing on-line condition monitoring strategies is clearly important to consider. For example, in this thesis, the gate current plateau and turn-on current switching rate have been identified to show clear temperature dependencies in SiC MOSFETs, however, the temperature sensitivity is shown to improve with reduced switching rates due to parasitic inductance. Since it is clearly not beneficial to drive SiC MOSFETs with increased switching losses for the purpose of enabling condition monitoring then intelligent gate drivers can be used to occasionally customise switching pulses on-line. Customising switching pulses in this context means reducing the switching rate to maximise the temperature sensitivity of the turn-on dI_{DS}/dt and gate current plateau. The design, implementation and evaluation of such a gate driver in a real time switching device is clearly a very important area of future work.

Bibliography

B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer, 2008.

J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices. Physics, Characteristics, Reliability*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2011.

A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors* 2nd ed.: SEMIKRON International GmbH, 2015.

The references are given in the References section of each chapter.

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A. Temperature Sensitivities

The nominal sensitivities of the Temperature Sensitive Electrical Parameters (TSEPs) characterised and studied in this thesis are summarised in this annex.

- **On-state voltage at low currents**

This TSEP has been analysed for SiC Schottky diodes, Si PiN diodes, Si IGBTs (at $V_{GS}=17$ V) and the body diode of a SiC MOSFET (at $V_{GS}=0$ V). For a sensing current of 50 mA, the results are summarised in Table B- 1. The evaluated temperatures are 25 °C and 150 °C.

Table B- 1 Temperature sensitivity of the on-state voltage at low currents for different technologies

Device	Part Number	Sensitivity (mV/°C)	Page
600 V/4 A SiC Schottky Diode	C3D0204A	-1.3	41
600 V/4 A Si PiN Diode	HFA04TB60	-1.9	44
1200 V/15 A Si IGBT	IGW15T120	-2.1	36
1200 V/10 A SiC MOSFET	C2M0280120D	-3.0	83

- **Threshold voltage**

The temperature sensitivity of the threshold voltage has been extracted from the datasheets for a Si IGBT and a SiC MOSFET. The results are summarised in Table B- 2.

Table B- 2 Temperature sensitivity of the threshold voltage for different technologies

Device	Part Number	Sensitivity (mV/°C)
1200 V/15 A Si IGBT	IGW15T120	-11
1200 V/24 A SiC MOSFET	CMF10120D	-5

- **Turn-on delay**

The impact of the threshold voltage is reflected on the time to threshold, as defined in chapter 2 of this thesis, generating a shift in time of the turn-on transient of the current. Table B- 3 shows the temperature sensitivity of the shift in time of the current during turn-on for a Si IGBT, a Si MOSFET and a SiC MOSFET. The evaluated temperatures

are 25 °C and 150 °C. The devices were driven using an external gate resistance of 47 Ω , gate driver voltage of 17 V and the DC link voltage was 200 V.

Table B- 3 Temperature sensitivity of the turn-on delay of the current for different technologies

Device	Part Number	Sensitivity (ps/°C)	Page
1200 V/15 A Si IGBT	IGW15T120	24	47
1200 V/24 A SiC MOSFET	CMF10120D	88	47
1200 V/20 A Si MOSFET	IXFX20N120P	216	47

- **Miller plateau duration of IGBTs**

The impact of the junction temperature on the duration of the Miller Plateau for IGBTs was presented in chapter 2. According to [1] it is also dependent on the DC link voltage and load current. The measurements in chapter 2 were done for a load current of 9 A and a DC link voltage of 200 V, using 100 Ω and 220 Ω gate resistances. The temperature sensitivities are summarised in Table B- 4. The evaluated temperatures are 25 °C and 150 °C.

Table B- 4 Temperature sensitivity of the Miller plateau duration of an IGBT

Device	Part Number	Gate Resistance (Ω)	Sensitivity (ps/°C)	Page
1200 V/15 A Si IGBT	IGW15T120	100	912	51
1200 V/15 A Si IGBT	IGW15T120	220	1256	52

- **dV_{CE}/dt during turn-off (IGBTs)**

The switching rate of the collector-emitter voltage during turn-off is also temperature dependent, as presented in chapter 2. According to [2] it is also dependent on the DC link voltage and load current. In chapter 2, it was characterised for a load current of 9 A and a DC link voltage of 200 V. The results are summarised in Table B- 5, using a gate driver voltage of 17 V and a gate resistance of 100 Ω . The evaluated temperatures are 25 °C and 150 °C.

Table B- 5 Temperature sensitivity of the switching rate of the collector-emitter voltage during turn-on of an IGBT (Gate resistance: 100 Ω)

Device	Part Number	Sensitivity (V/ μ s·°C)	Page
1200 V/15 A Si IGBT	IGW15T120	-2.856	51

- **Turn-off delay**

The impact of the junction temperature on delay of the turn-off current was presented in chapter 2 for IGBTs and in chapter 3 for silicon and silicon carbide MOSFETs. According to [3], where it is analysed and characterised for silicon IGBTs, it is also dependent on the DC link voltage and load current. The measurements in chapter 2 and chapter 3 were done for a load current of 9 A and a DC link voltage of 200 V, using 100 Ω gate resistances. The temperature sensitivities are summarised in Table B- 6. The evaluated temperatures are 25 °C and 150 °C.

Table B- 6 Temperature sensitivity of the turn-off delay of the current for different technologies (Gate resistance: 100 Ω)

Device	Part Number	Sensitivity (ps/°C)	Page
1200 V/15 A Si IGBT	IGW15T120	1328	85
1200 V/24 A SiC MOSFET	CMF10120D	544	86
1200 V/20 A Si MOSFET	IXFX20N120P	2496	85

In the case of the SiC MOSFET the temperature sensitivity is lower because of the lower parasitic capacitances compared with the silicon IGBT and the silicon MOSFET. The temperature sensitivity can be improved if the transient is slowed down by means of increasing the gate resistance, as the results in Table B- 7 show, for a gate resistance of 220 Ω . The evaluated temperatures are 25 °C and 150 °C.

Table B- 7 Temperature sensitivity of the turn-off delay of the current of a SiC MOSFET (Gate resistance: 220 Ω)

Device	Part Number	Sensitivity (ps/°C)	Page
1200 V/24 A SiC MOSFET	CMF10120D	1232	86

- **Reverse recovery of silicon PiN diodes**

The impact of the junction temperature on the reverse recovery of silicon PiN diodes was presented in chapter 2 and it was compared with the reverse recovery of a silicon carbide Schottky in chapter 3. According to [4, 5] it is also dependent on the DC link voltage, the switching rate during turn-on of the complementary device and the forward current. The measurements in chapter 3 were done for a load current of 18 A and a DC link voltage of 200 V, using a 150 Ω gate resistance. The temperature sensitivity of

the peak reverse recovery current is shown in Table B- 8. The evaluated temperatures are 25 °C and 100 °C.

Table B- 8 Temperature sensitivity of the peak reverse recovery current of a PiN diode

Device	Part Number	Sensitivity (mA/°C)	Page
600 V/15 A Si PiN diode	15ETH06	-23.5	79

The switching rate of the reverse recovery current is also temperature dependent. In the case of the evaluated Si PiN diode it increases with temperature [6]. The temperature sensitivity is shown in Table B- 9. The evaluated temperatures are 25 °C and 100 °C.

Table B- 9 Temperature sensitivity of the switching rate of the reserve recovery current of a PiN diode

Device	Part Number	Sensitivity (V/μs·°C)	Page
600 V/15 A Si PiN diode	15ETH06	0.893	79

• Gate current transient of SiC MOSFETs

The impact of the junction temperature on the gate transient for SiC MOSFETs was presented as TSEP in chapter 3. The time when the gate current plateau occurs and the value of the gate current plateau are TSEPs. Both are dependent on the load current, as shown in chapter 3, hence its use as TSEP would require decoupling the effects of the load current and temperature. The temperature sensitivities of the gate current transient of a 1200 V/42 A SiC MOSFET for a load current of 9 A, DC link voltage of 200 V, gate voltage of 17 V and gate resistance of 220 Ω are shown in Table B- 10 and Table B- 11. The evaluated temperatures are 25 °C and 150 °C.

Table B- 10 Temperature sensitivity of the *gate current plateau* of a SiC MOSFET during turn-on

Device	Part Number	Sensitivity (μA/°C)	Page
1200 V/42 A SiC MOSFET	CMF20120D	64	109

Table B- 11 Temperature sensitivity of the *time to gate current plateau* of a SiC MOSFET during turn-on

Device	Part Number	Sensitivity (ps/°C)	Page
1200 V/42 A SiC MOSFET	CMF20120D	792	109

- **Switching rate of the current during turn-on (SiC MOSFETs)**

The impact of the junction temperature on the switching rate of the current of a SiC MOSFET during turn-on (dI_{DS}/dt) was presented and analysed thoroughly on chapter 3 and chapter 4, where its dependencies and the nominal and relative temperature sensitivities were characterised. The nominal temperature sensitivities of dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET for a load current of 14 A, DC link voltage of 600 V, gate voltage of 20 V and gate resistances of 47 Ω and 220 Ω are shown in Table B- 12. The evaluated temperatures are 50 °C and 150 °C.

Table B- 12 Temperature sensitivity of the switching rate of the current of a SiC MOSFET during turn-on

Device	Part Number	Gate Resistance (Ω)	Sensitivity ($A/\mu s \cdot ^\circ C$)	Page
1200 V/42 A SiC MOSFET	CMF20120D	47	0.24	161
1200 V/42 A SiC MOSFET	CMF20120D	220	0.10	162

- **On-state resistance of a MOSFET**

The impact of the junction temperature on the on-state resistance of a MOSFET was presented on chapter 3 and chapter 4, where its dependency on the gate-source voltage was evaluated. It was analysed for a silicon MOSFET, a silicon superjunction MOSFET (COOLMOS) and silicon carbide MOSFETs of different generations. For a sensing current of 50 mA and a gate-source voltage of 20 V, the nominal temperature sensitivities are summarised in Table B- 13. The evaluated temperatures are 22°C and 125 °C.

Table B- 13 Temperature sensitivity of the on-state resistance of different MOSFET technologies

Device	Part Number	Sensitivity ($m\Omega/^\circ C$)	Page
1200 V/20 A Si MOSFET	IXFX20N120P	6.38	151
900 V/15 A COOLMOS	IPW90R340C3	2.80	151
1200 V/24 A SiC MOSFET (G1)	CMF10120D	0.42	151
1200 V/19 A SiC MOSFET (G2)	C2M0160120D	0.69	155

References

- [1] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5122-5132, 2016.
- [2] A. Bryant, S. Yang, P. Mawby, D. Xiang, L. Ran, P. Tavner, *et al.*, "Investigation into IGBT dV/dt during turn-off and its temperature dependence," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3019-3031, 2011.
- [3] V. K. Sundaramoorthy, E. Bianda, R. Bloch, D. Angelosante, I. Nistor, G. J. Riedel, *et al.*, "A study on IGBT junction temperature (T_j) online estimation using gate-emitter voltage (V_{GE}) at turn-off," *Microelectronics Reliability*, vol. 54, no. 11, pp. 2423-2431, 2014.
- [4] H. Luo, Y. Chen, W. Li, and X. He, "Online High-Power p-i-n Diode Junction Temperature Extraction With Reverse Recovery Fall Storage Charge," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2558-2567, 2017.
- [5] H. Luo, W. Li, and X. He, "Online high-power P-i-N diode chip temperature extraction and prediction method with maximum recovery current di/dt ," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2395-2404, 2015.
- [6] R. Bürkel and T. Schneider. *Fast Recovery Epitaxial Diodes (FRED) Characteristics - Applications - Examples. IXAN0044*. Available: <http://www.ixys.com/Documents/AppNotes/IXAN0044.pdf> (Access: 5/07/2017).

B. Technical Drawings

This annex includes the technical drawings of the press-pack prototype:

Drawing 1: Base

Drawing 2: Anode Contact

Drawing 3: Cathode Contact

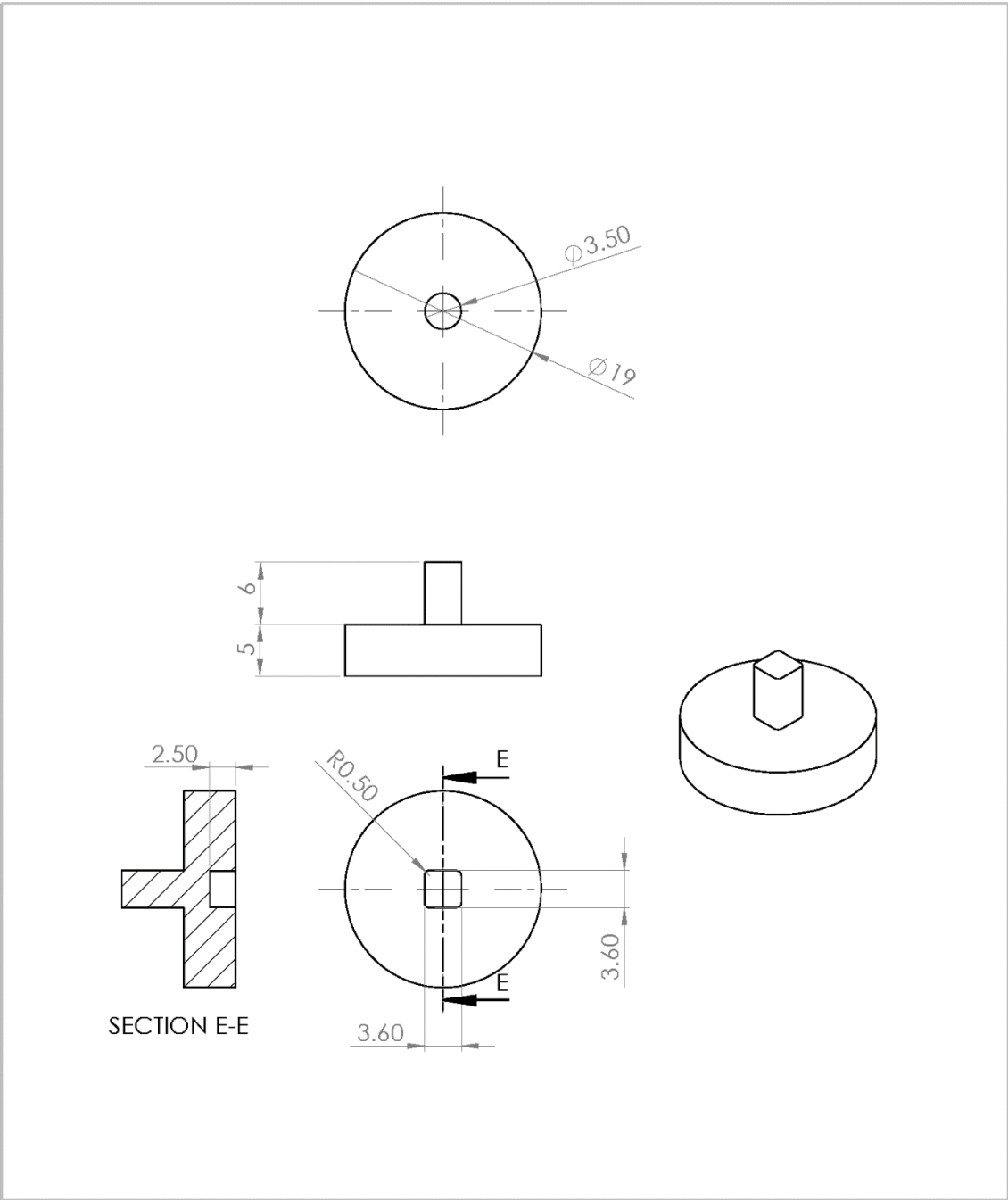
Drawing 4: Top Pole

Drawing 5: Die Carrier

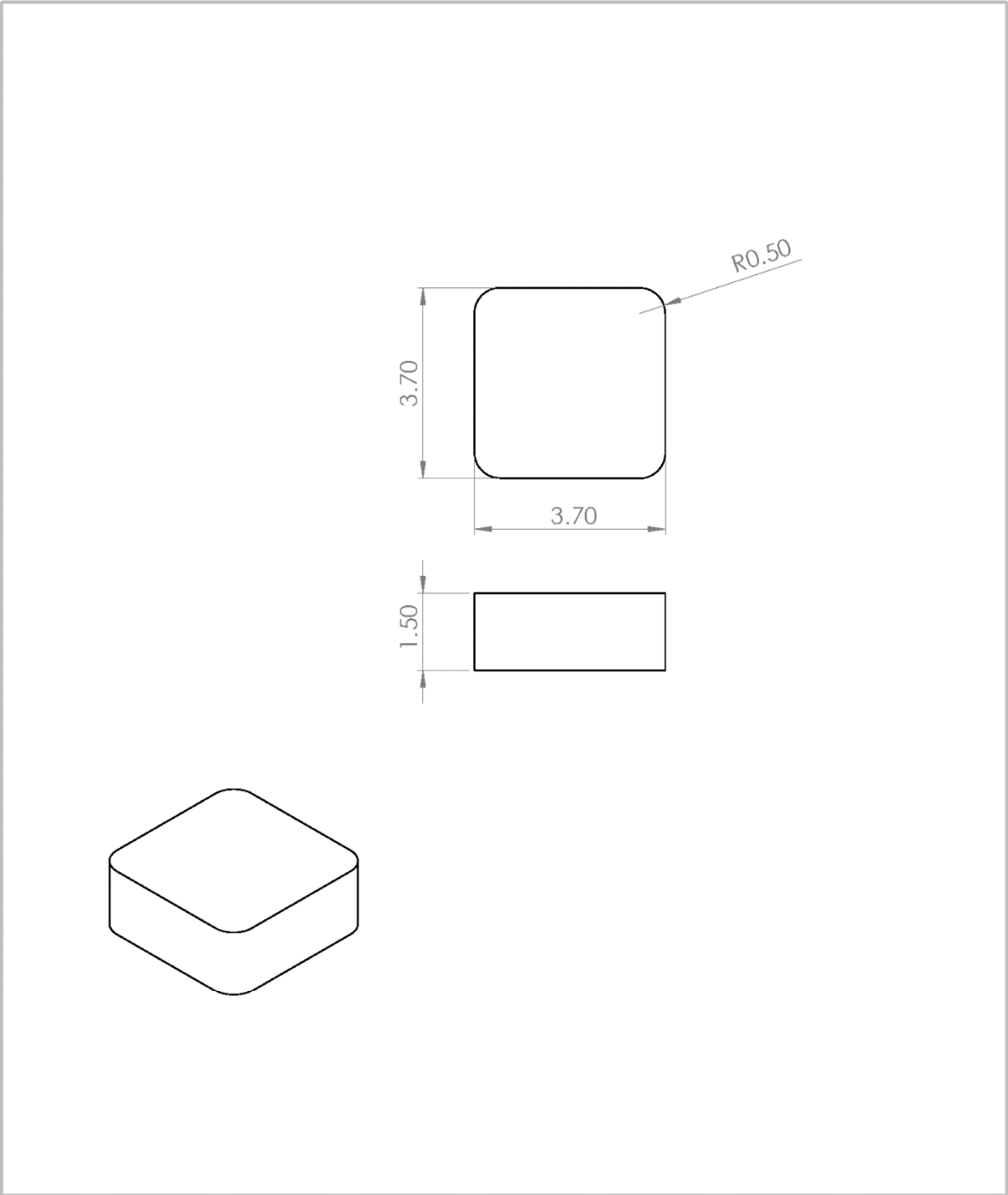
Drawing 6: Case

Drawing 7: Base 4 diodes

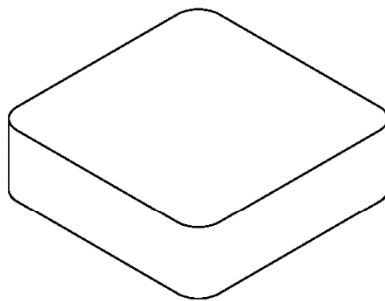
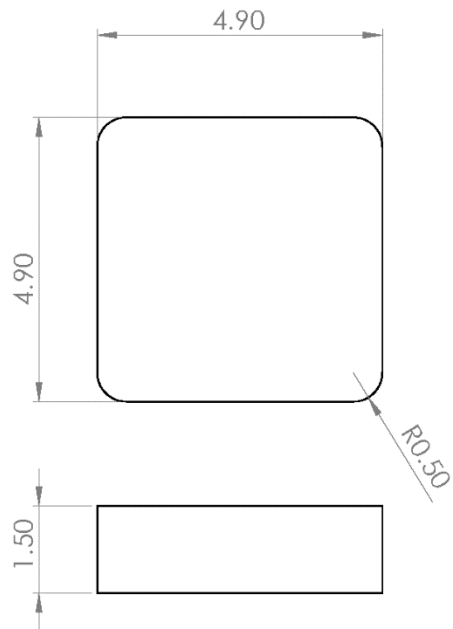
Drawing 8: Case 4 diodes



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CHK'D														
APP'Y'D														
MFG														
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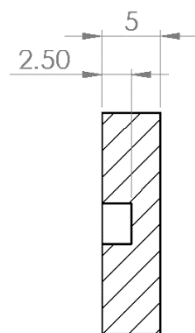


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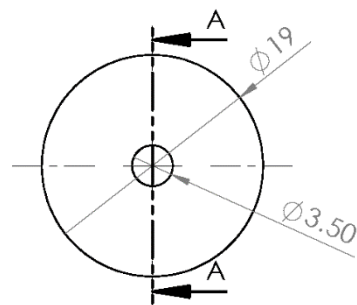


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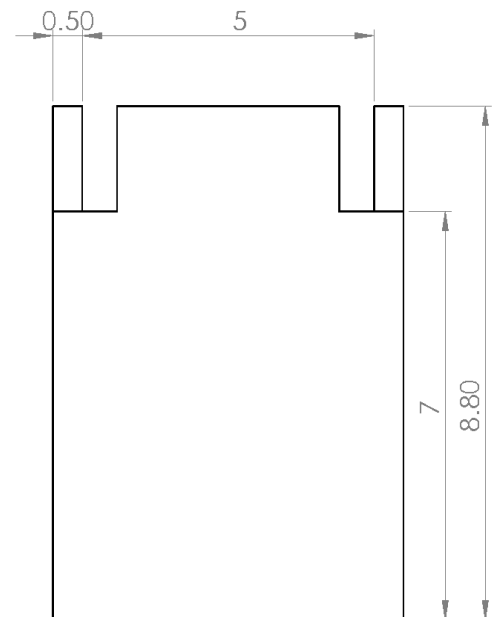
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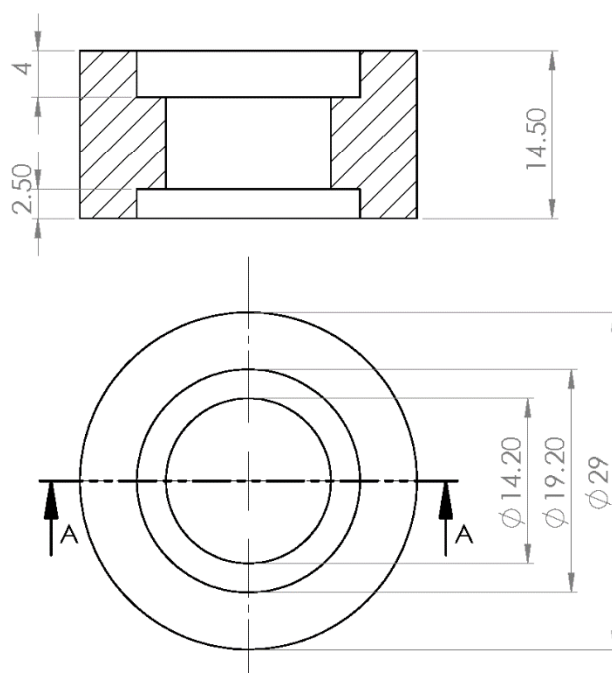
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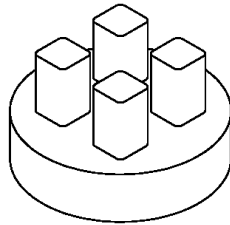
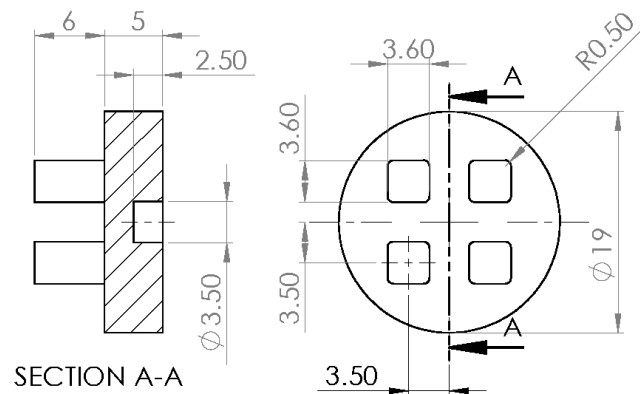
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						WEIGHT:		SCALE: NO SCALE		SHEET 1 OF 1	



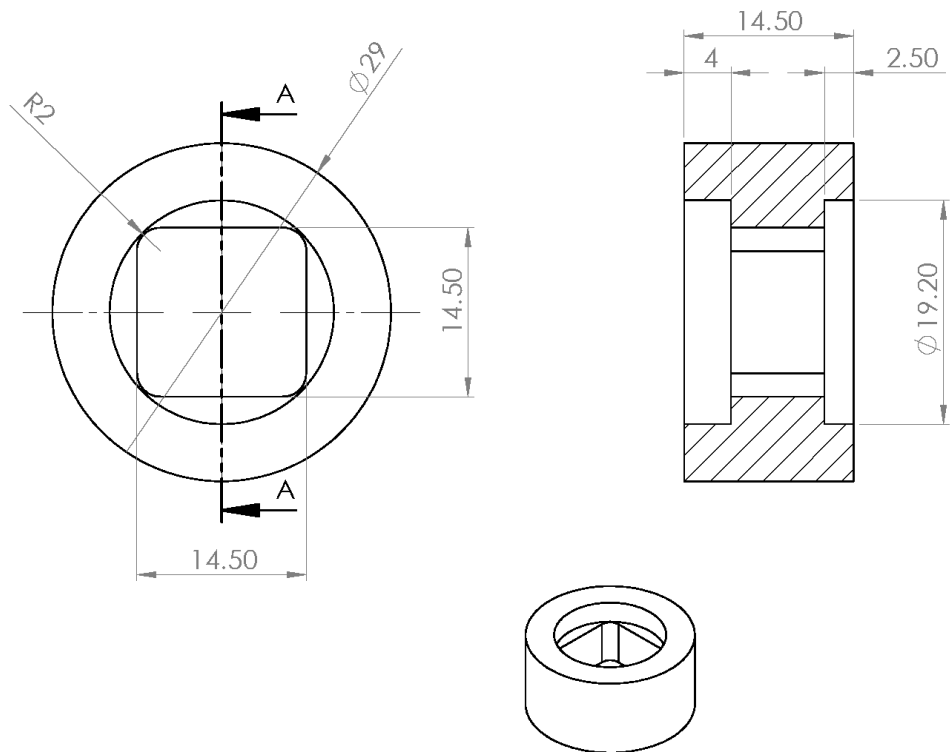
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:				FINISH:		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION	
								University of Warwick			
	NAME	SIGNATURE	DATE					TITLE: Die Carrier			
DRAWN											
CHK'D											
APP'VD											
MFG											
Q.A				MATERIAL: PPS				DWG NO. 5		A4	
				WEIGHT:				SCALE: NO SCALE		SHEET 1 OF 1	



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:				FINISH:		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION	
								<div>University of Warwick</div>			
		NAME		SIGNATURE		DATE				<div>TITLE:</div> <div>Case</div>	
DRAWN											
CHK'D											
APP'VD											
MFG											
Q.A											
						MATERIAL: PEEK		DWG NO.		6	
										A4	
						WEIGHT:		SCALE: NO SCALE		SHEET 1 OF 1	



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:		FINISH: Ni plating - 5u		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION	
						University of Warwick			
						TITLE: Base 4 diodes			
DRAWN		NAME		SIGNATURE		DATE		DWG NO.	
CHK'D								7	
APPVD								A4	
MFG									
Q.A									
						MATERIAL: Copper			
						WEIGHT:		SCALE: NO SCALE	
								SHEET 1 OF 1	



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:		FINISH:		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION	
						<div>TITLE:</div> <div>Case 4 diodes</div>			
DRAWN		NAME	SIGNATURE	DATE			DWG NO.		8
CHK'D									
APP'VD									
MFG									
Q.A					MATERIAL:				A4
					PEEK/PPS				
					WEIGHT:		SCALE: NO SCALE		SHEET 1 OF 1